ACADEMIC REGULATIONS
COURSE STRUCTURE
AND
DETAILED SYLLABUS

M. Tech.
EMBEDDED SYSTEMS

(Applicable for the batches admitted from 2011-2012)

VNR VIGNANA JYOTHI
INSTITUTE OF ENGINEERING & TECHNOLOGY
(AFFILIATED TO JNTUH)
An Autonomous Institute under JNTUH

Bachupally, Nizampet (S.O), Hyderabad –500090
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Academic Regulations 2011 For M.Tech. Degree Course
(Effective for the students admitted into first year from the academic year 2011-2012)

1. Introduction

Academic Programmes of the institute are governed by rules and regulations as approved by the academic council of the institute.

These academic rules and regulations are effective from the academic year 2011-12, for the students admitted into two year post graduate programme offered by the college leading to Master Of Technology (M. Tech.) degree in the disciplines viz., Civil Engineering, Electrical and Electronics Engineering, Mechanical Engineering, Electronics and Communication Engineering, Computer science and Engineering, Information Technology, Electronics and Instrumentation Engineering and Automobile Engineering.

The M.Tech. Degree of Jawaharlal Nehru Technological University Hyderabad shall be conferred on candidates who are admitted to the program after fulfilling all the requirements for the award of the Degree.

1.1 Eligibility for Admissions

Admission to the above program shall be made subject to the eligibility, qualifications and specialization prescribed by the University from time to time. Admissions shall be made on the basis of GATE Rank and merit rank obtained by the qualifying candidate at an Entrance Test conducted by the University, subject to reservations prescribed by the university/ State Government from time to time.

2. Courses of Study

The following specializations are offered at present for the M.Tech. Course of study.

1. Advanced Manufacturing Systems
2. Highway Engineering
3. Structural Engineering
4. Power Electronics
5. Software Engineering
6. VLSI System Design
7. Embedded Systems
8. Geotechnical Engineering
9. Electronic Instrumentation
10. Automation

and any other course as approved by the Academic Council of the Institute and the authorities of the University from time to time.

2.1 Departments offering M.Tech. Programmes with specializations are mentioned below:

ME	1.Advanced Manufacturing Systems 2. Automation
CE	1. Highway Engineering 2.Structural Engineering 3 Geotechnical Engineering
EEE	Power Electronics
CSE	Software Engineering
ECE	1.VLSI System Design 2.Embedded Systems
EIE	Electronic Instrumentation

3. Attendance

Each academic year shall be divided into two semesters, each of 90 Instructions days, excluding examination, evaluation, declaration of results etc.

3.1 A candidate shall be deemed to have eligibility to write end semester examinations in a subject if he has put in at least 75% of attendance in that subject.

3.2 Shortage of attendance up to 10% in any subject (i.e. 65% and above and below 75%) may be condoned by the College Academic Committee on genuine and valid reasons on application by the candidate with supporting evidence.

3.3 A candidate shall get minimum required attendance at least in three (3) theory subjects in the present semester to get promoted to the next semester. In order to qualify for the award of the M.Tech. Degree, the candidate shall complete all the academic requirements of the subjects, as per the course structure.

3.4 Shortage of attendance below 65% shall in no case be condoned.

3.5 A stipulated fee shall be payable towards condonation of shortage of attendance.

3.6 In case the candidate secures less than the required attendance in any subject(s), he shall not be permitted to appear for the End Examination in that subject(s). He shall re-register the subject when next offered.

4. Evaluation

The performance of the candidate in each semester shall be evaluated subject-wise, with a maximum of 100 marks for theory and 100 marks for practicals, on the basis of Internal Evaluation and End Semester Examination.

4.1 For the theory subjects 60 marks shall be awarded based on the performance in the End Semester Examination, 40 marks shall be awarded based on the Internal Evaluation. The internal evaluation shall be made based on the better of the marks secured in the two Mid Term-Examinations conducted one in the middle of the Semester and the other immediately after the completion of instruction. Each mid term examination shall be conducted for duration of 2 Hours with 4 questions to be answered out of 6 questions.

4.2 For practical subjects, 60 marks shall be awarded based on the performance in the End Semester Examinations, 40 marks shall be awarded based on the day-to-day performance as Internal Marks.

4.3 There shall be two seminar presentations during the I year, one in each semester. For seminar, a student under the supervision of a faculty member, shall collect the literature on a topic and critically review the literature and submit it to the Department in a report form and shall make an oral presentation before the Departmental Committee. The Departmental Committee consists of Head of the Department, supervisor and two other senior faculty members of the department. For each Seminar there will be only internal evaluation of 50 marks. A candidate has to secure a minimum of 50% to be declared successful.

4.4 There shall be a Comprehensive Viva-Voce in II year I Semester. The Comprehensive Viva-Voce will be conducted by a Committee consisting of Head of the Department and two Senior Faculty members of the Department. The Comprehensive Viva-Voce is aimed to assess the students' understanding in various subjects studied during the M.Tech. course of study. The Comprehensive Viva-Voce is valued for 100 marks by the Committee. There are no internal marks for the Comprehensive viva-Voce.

4.5 A candidate shall be deemed to have secured the minimum academic requirement in a subject if he secures a minimum of 40% of marks in the End Examination and a minimum aggregate of 50% of the total marks in the End Semester Examination and Internal Evaluation taken together.

4.6 A candidate shall be given one chance to re-register for each subject provided the internal marks secured by a candidate are less than 50% and he has failed in the end examination. In such a case candidate may re-register for the subject(s) and secure required minimum attendance. Attendance in the re-registered subject(s) has to be calculated separately to become eligible to write the end examination in the re-registered subject(s). Re-registration for the subjects is allowed only if that particular re-registration subjects are the hindrance for the award of Degree. Re-registration is allowed in this case provided the student doesn't have any subject(s) yet to pass other than the re-registration subjects with prior permission.

4.7 Laboratory examination for M.Tech. courses must be conducted with two Examiners, one of them being Laboratory Class Teacher and second examiner shall be a teacher of same specialization either external or from the same dept.

5. Evaluation of Project / Dissertation Work.

5.1 Registration of Project Work: A candidate is permitted to register for the project work after satisfying the attendance requirement of all the subjects (theory and practical subjects).

5.2 A Project Review Committee (PRC) shall be constituted with at least four members namely HOD, PG Coordinator of the Department, project supervisor and one senior faculty member of same specialization.

5.3 After satisfying 5.1, a candidate has to submit, in consultation with the project supervisor, the title, objective and plan of action of his project work to the Departmental Academic Committee for its approval. Only after obtaining the approval of Departmental Academic Committee, the student can initiate the Project work.

5.4 If a candidate wishes to change his supervisor or topic of the project he can do so with the approval of Departmental Academic Committee. However, the Departmental Committee shall examine whether the change of topic/supervisor leads to a major change of his initial plans of project proposal. If so, his date of registration for the project work starts from the date of change of Supervisor or topic as the case may be.

5.5 Internal Evaluation of the project shall be on the basis of the seminars(Project reviews) conducted during the II year by the committee consisting of Head of the Department, project supervisor ,PG coordinator of the Department and senior faculty member of the Department. belonging to same specialization. A candidate shall submit status report in a spiral bound copy form.

5.6 The work on the project shall be initiated in the beginning of the second year and the duration of project is for two semesters. A candidate is permitted to submit Project Thesis only after successful completion of theory and practical course with the approval of PRC not earlier than 240 days from the date of registration of the project work. For the approval of PRC the candidate shall submit the daft copy of thesis to the Head of the Department (Through project supervisor/PG coordinator) and shall make an oral presentation before the PRC.

5.7 After approval of PRC, every student has to submit three copies of the Project Thesis certified by the supervisor to the Department.

5.8 The thesis shall be adjudicated by one examiner selected by the Chief Superintendent. For this, HOD shall submit a panel of 3/ 5 examiners, who are eminent in that field with the help of the concerned guide.

5.9 If the report of the examiner is not favourable, the candidate shall revise and resubmit the Thesis, within the time frame as described by PRC. If the report of the examiner is unfavourable again, the thesis shall be summarily rejected.

5.10 If the report of the examiner is favorable, viva-voce examination shall be conducted by a board consisting of the supervisor, Head of the Department and the examiner who adjudicated the Thesis. The Board shall jointly report candidates work as:

A. Excellent
B. Good
C. Satisfactory
D. Unsatisfactory

Head of the Department shall coordinate and make arrangements for the conduct of viva-voce examination. The candidate has to secure any one of the grades as Excellent, Good or Satisfactory on his thesis/dissertation and viva-voce. If the report of the viva-voce is unsatisfactory, the candidate will retake the viva-voce examination after three months. If he fails to get a satisfactory report at the second viva-voce examination, he has to reregister the project work as in clause 5.1. However, the candidate may select a new guide and new topic with the approval of the PRC and submit the project report with a minimum of 240 days from the date of re-registration. Of course this shall not prejudice the clause 6.1 below. The candidate can be permitted to change the topic/guide only once.

6. Award of Degree and Class

A student shall be declared eligible for the award of the M.Tech. degree, if he pursues a course of study and completes it successfully for not less than two academic years and not more than four academic years.

6.1 A student, who fails to fulfil all the academic requirements for the award of the degree within four academic years from the year of his admission, for any reason whatsoever, shall forfeit his seat in M.Tech. Course.

6.2 After a student has satisfied the requirements prescribed for the completion of the program and is eligible for the award of M. Tech. Degree shall be placed in one of the following four classes:

Class Awarded	% of marks to be secured
First Class with Distinction	70% and above
First Class	Below 70% but not less than 60%
Second Class	Below 60% but not less than 50%

(The marks in internal evaluation and end examination shall be shown separately in the marks memorandum)

7. Withholding of Results

If the candidate has not paid any dues to the Institute or if any case of indiscipline is pending against him, the result of the candidate will be withheld and he will not be allowed into the next higher semester. The issue of the degree is liable to be withheld in such cases. This delay shall not prejudice clauses Nos.6.0 and 6.1

8. Transitory Regulations

Candidate who have discontinued or have been detained for want of attendance or who have failed after having undergone the course are eligible for admission to the same or equivalent subjects as and when subjects are offered without precluding clauses Nos.6.0 and 6.1

9. General

9.1 The academic regulations should be read as a whole for purpose of any interpretation.

9.2 In case of any doubt or ambiguity in the interpretation of the above rules, the decision of the Principal is final.

9.3 The Institute may change or amend the academic regulations and syllabi at any time and the changes and amendments made shall be applicable to all the students with effect from the date notified by the Institute.

9.4 Wherever the words he, him or his occur, they will also include she, her and hers.

10. Supplementary Examination

Supplementary examinations will be conducted along with regular semester end examinations. Supplementary examinations will be conducted to a maximum number of four continuous times subsequent to the revision of the syllabus. Supplementary examinations will be conducted in the equivalent courses as approved by the Institute Academic Committee.

VNR VIGNANA JYOTHI INSTITUTE OF ENGINEERING & TECHNOLOGY, HYDERABAD
M.Tech. (EMBEDDED SYSTEMS)

I YEAR I SEMESTER **COURSE STRUCTURE**

Subject Code	Subject Name	Lectures	P	Credits
R11ESS2101	Microcontrollers for Embedded System Design	3	0	3
R11ESS2102	Embedded Real Time Operating Systems	3	0	3
R11VSD2102	VLSI Technology & Design	3	0	3
R11ESS2103	Advanced Computer Networks	3	0	3
R11ESS2107 R11ESS2108 R11ESS2109	Elective – I Advanced Computer Architecture Wireless LANs & PANs Advanced Digital Signal Processing	3	0	3
R11VSD2107 R11ESS2110 R11ESS2111	Elective – II Digital System Design Neural Networks & Applications Advanced Operating Systems	3	0	3
R11VSD2201	Embedded System Lab – I	0	3	2
R11ESS2301	Seminar	0	0	2
Total		**18**	**3**	**22**

I YEAR II SEMESTER **COURSE STRUCTURE**

Subject Code	Subject Name	Lectures	P	Credits
R11ESS2104	Hardware Software Co-Design	3	0	3
R11ESS2105	Digital Signal Processors and Architectures	3	0	3
R11ESS2106	System Modeling and Simulation	3	0	3
R11VSD2101	CPLD & FPGA Architectures and Applications	3	0	3
R11VSD2112 R11ESS2112 R11ESS2113	Elective – III Low power VLSI Design Robotics Ad-Hoc Wireless	3	0	3
R11VSD2110 R11VSD2104 R11ESS2114	Elective – IV Image & Video Processing System On Chip Architecture Network Security & Cryptography	3	0	3
R11ESS2202	Embedded Systems Lab – II using pSoC	0	3	2
R11ESS2302	Seminar	0	0	2
Total		**18**	**3**	**22**

*** P: Practical**

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M. Tech. (EMBEDDED SYSTEMS)

II YEAR I SEMESTER **COURSE STRUCTURE**

Subject Code	Subject Name	Lectures	T/P/D	Credits
R11ESS2303	Comprehensive viva	0	0	2
R11ESS2304	Project Seminar - I	0	3	2
R11ESS2305	Project work	0	0	18
Total		**0**	**3**	**22**

II YEAR II SEMESTER **COURSE STRUCTURE**

Subject Code	Subject Name	Lectures	T/P/D	Credits
R11ESS2306	Project work	0	0	20
R11ESS2307	Project Seminar - II	0	0	2
Total Credits		0	0	22

- P: Practical

VNR VIGNANA JYOTHI INSTITUTE OF ENGINEERING & TECHNOLOGY, HYDERABAD

I Year – I Sem. M.Tech. (Embedded Systems)	**L**	**T/P/D**	**C**
	3	**0**	**3**

(R11ESS2101) MICROCONTROLLERS FOR EMBEDDED SYSTEM DESIGN

Unit – I: Introduction to Embedded Systems

Overview of Embedded Systems, Processor Embedded into a system, Embedded Hardware Units and Devices in system, Embedded Software, Complex System Design, Design Process in Embedded System, Formalization of System Design, Classification of Embedded Systems.

Unit – II: Microcontrollers and Processor Architecture & Interfacing

8051 Architecture, Input/Output Ports and Circuits, External Memory, Counters and Timers, PIC Controllers. Interfacing Processor (8051, PIC), Memory Interfacing, I/O Devices, Memory Controller and Memory arbitration Schemes.

Unit – III: Embedded RISC Processors & Embedded System-on Chip Processor

PSOC (Programmable System-on-Chip) architectures, Continuous Timer blocks, Switched Capacitor blocks, I/O blocks, Digital blocks, Programming of PSOC, Embedded RISC Processor architecture – ARM Processor architecture, Register Set, Modes of operation and overview of Instructions

Unit – IV: Interrupts & Device Drivers

Exceptions and Interrupt handling Schemes – Context & Periods for Context Switching, Deadline & interrupt latency. Device driver using Interrupt Service Routine, Serial port Device Driver, Device drivers for Internal Programmable timing devices

Unit – V: Network Protocols

Serial communication protocols, Ethernet Protocol, SDMA, Channel & IDMA, External Bus Interface

TEXT BOOKS:

1. Embedded Systems - Architecture Programming and Design – Raj Kamal, 2nd ed., 2008,TMH.
2. PIC Microcontroller and Embedded Systems – Muhammad Ali Mazidi, Rolin D.Mckinaly, Danny Causy – PE.
3. Designers Guide to the Cypress PSOC – Robert Ashpy, 2005, Elsevier.

REFERENCES:

1. Embedded Microcomputer Systems, Real Time Interfacing – Jonathan W. Valvano – Brookes / Cole, 1999, Thomas Learning.
2. ARM Systems Developers Guides- Design & Optimizing System Software - Andrew N. Sloss, Dominic Symes, Chris Wright, 2004, Elsevier.
3. Designing with PIC Microcontrollers- John B. Peatman, 1998, PH Inc.

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I Year – I Sem. M.Tech. (Embedded Systems)	**L**	**T/P/D**	**C**
	3	**0**	**3**

(R11ESS2102) EMBEDDED REAL TIME OPERATING SYSTEMS

Unit – I: Introduction

Introduction to UNIX, Overview of Commands, File I/O,(open, create, close, lseek, read, write), Process Control (fork, vfork, exit, wait, waitpid, exec), Signals, Interprocess communication,(pipes, fifos, message queues, semaphores, shared memory)

Unit II: Real Time Systems:

Typical real time applications, Hard Vs Soft real-time systems, A reference model of Real Time Systems: Processors and Resources, Temporal Parameters of real Time Work load, Periodic task model precedence constraints and data dependency, functional parameters, Resource Parameters of jobs and parameters of resources.

Unit III: Scheduling & Inter-process Communication

Commonly used Approaches to Real Time Scheduling Clock Driven, Weighted Round Robin, Priority Driven, Dynamic Vs State Systems, Effective release time and Dead lines, Offline Vs Online Scheduling.

Inter-process Communication and Synchronization of Processes, Tasks and Threads- Multiple Process in an Application, Problem of Sharing data by multiple tasks & routines, Inter-process communication

Unit IV: Real Time Operating Systems & Programming Tools

Operating Systems Services, I/O Subsystems, RT & Embedded Systems OS, Interrupt Routine in RTOS Environment

Micro C/OS-II- Need of a well Tested & Debugged RTOs, Use of μCOS-II

Unit V: VX Works & Case Studies

Memory managements task state transition diagram, pre-emptive priority, Scheduling context switches- semaphore- Binary mutex, counting watch dugs, I/O system

Case Studies of programming with RTOS- Case Study of Automatic Chocolate Vending m/c using μCOS RTOS, case study of sending application Layer byte Streams on a TCP/IP network, Case Study of an Embedded System for a smart card.

TEXT BOOKS:

1. Embedded Systems- Architecture, Programming and Design by Rajkamal, 2nd ed., 2008,TMH.
2. Real Time Systems- Jane W. S. Liu- PHI.
3. Real Time Systems- C.M.Krishna, KANG G. Shin, 1996, TMH

REFERENCES:

1. Advanced UNIX Programming, Richard Stevens
2. VX Works Programmers Guide

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I Year – I Sem. M.Tech. (Embedded Systems)	**L**	**T/P/D**	**C**
	3	**0**	**3**

(R11VSD2102) VLSI TECHNOLOGY & DESIGN

UNIT – I:

Review of Microelectronics and Introduction to MOS Technologies: MOS, CMOS, BiCMOS Technology, Trends And Projections.

Basic Electrical Properties of MOS, CMOS & BiCMOS Circuits: I_{ds}-V_{ds} relationships, Threshold Voltage V_t, G_m, G_{ds} and ω_o, Pass Transistor, MOS, CMOS & Bi CMOS Inverters, Zpu/Zpd, MOS Transistor circuit model, Latch-up in CMOS circuits.

UNIT – II:

LAYOUT DESIGN AND TOOLS: Transistor structures, Wires and Vias, Scalable Design rules, Layout Design tools.

LOGIC GATES & LAYOUTS: Static Complementary Gates, Switch Logic, Alternative Gate circuits, Low power gates, Resistive and Inductive interconnect delays.

UNIT – III:

COMBINATIONAL LOGIC NETWORKS: Layouts, Simulation, Network delay, Interconnect design, Power optimization, Switch logic networks, Gate and Network testing.

UNIT –IV:

SEQUENTIAL SYSTEMS: Memory cells and Arrays, Clocking disciplines, Design, Power optimization, Design validation and testing.

UNIT – V:

FLOOR PLANNING & ARCHITECTURE DESIGN: Floor planning methods, off-chip connections, High-level synthesis, Architecture for low power, SOCs and Embedded CPUs, Architecture testing.

TEXT BOOKS:

1. Essentials of VLSI Circuits and Systems, K. Eshraghian Eshraghian. D, A.Pucknell, 2005, PHI.
2. Modern VLSI Design - Wayne Wolf, 3rd ed., 1997, Pearson Education.

REFERENCES:

1. Principals of CMOS VLSI Design – N.H.E Weste, K.Eshraghian, 2nd ed., Adisson Wesley.

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I Year – I Sem. M.Tech. (Embedded Systems)	**L**	**T/P/D**	**C**
	3	**0**	**3**

(R11 ESS 2103) ADVANCED COMPUTER NETWORKS

Unit -I: Congestion and Quality of Service (QoS)
Data traffic, Congestion, Congestion Control, Open loop and Closed Loop Congestion Control in TCP and Frame Relay, Quality of Service, Flow Characterization, Flow Classes, Need For QoS, Resource Allocation, Best Effort Service Features, Techniques to Improve QoS.

Queue Management: Passive, Active (RED), and Fair (BRED, Choke) Queue Management Schemes, Scheduling, Traffic Shaping, Resource Reservation and Admission Control Scheduling, Integrated and Differential Services.

Unit-II:
Wireless Local Area Networks: Introduction, Wireless LAN Topologies, Wireless LAN Requirements, the Physical Layer, the Medium Access Control (MAC) Layer, Latest Developments.

Wireless Personal Area Networks (WPANs): Introduction to PAN Technology and Applications, Commercial Alternatives- Bluetooth, Home RF.

Wireless Wide Area Networks and MANS: The Cellular Concept, Cellular Architecture, The First-Generation Cellular Systems, The Second- Generation Cellular Systems, The Third- Generation Cellular Systems, Wireless in Local Loop, Wireless ATM, IEEE 802.16 Standard.

Unit-III:
Cellular Systems and Infrastructure- Based Wireless Networks: Cellular Systems Fundamentals, Channel Reuse, SIR and User Capacity, Interference Reduction Techniques, Dynamic Resource Allocation, Fundamental Rate Limits.

Virtual Private Network (VPN): Types of VPN, VPN General Architecture, Current VPN Advantages and Disadvantages, VPN Security Issues, VPN Standards.

Unit-IV:
ATM Protocol Reference Model: Introduction, Transmission Convergence (TC) Sub-layer, Physical Medium Dependent (PMD) Sub-layer, Physical Layer Standards for ATM.

ATM Layer: ATM Cell Header Structure at UNI, ATM Cell Header Structure at NNI, ATM Layer Functions.

ATM Adaptation Layer: Service Classes and ATM Adaptation Layer, ATM Adaptation Layer 1 (AAL1), ATM Adaptation Layer 2 (AAL2), ATM Adaptation Layer 3/4 (AAL3/4), ATM Adaptation Layer 5 (AAL5).

ATM Traffic and Service Parameterization: ATM Traffic Parameters, ATM Service Parameters, Factors Affecting QoS Parameters, ATM Service Categories, QoS and QoS Classes.

Unit-V:
Interconnection Networks: Introduction, Banyan Networks- Properties, Crossbar Switch, Three Stage Class Networks, Rearrangeable Networks, Folding Algorithm, Benes Networks, Looping Algorithm, Bit- Allocation Algorithm.

SONET/SDH: SONET/SDH Architecture, SONET Layers, SONET Frames, STS Multiplexing, SONET Networks.

TEXT BOOKS:

1. Wireless Communications - Andrea Goldsmith, 2005, Cambridge University Press.
2. Ad Hoc Wireless Networks: Architectures and Protocols - C. Siva Ram Murthy and B.S.Manoj, 2004, PHI.
3. Data Communication and Networking - B. A.Forouzan, 2nd updating, 2004,TMH

REFERENCES:

1. Introduction to Broadband Communication Systems- Sadiku, Mathew N.O., Akujuobi, Cajetan.M, PHI
2. Wireless Networks- P. Nicopolitidis, A. S. Pomportsis, G. I. Papadimitriou, M. S. Obaidat, 2003, JohnWiley & Sons
3. High Performance TCP / IP Networking – Mahaboob Hassan, Jain Raj, PHI.
4. Telecommunication System Engineering – Roger L. Freeman, 4/ed., Wiley-Interscience, John Wiley & Sons, 2004.

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I Year – I Sem. M.Tech. (Embedded Systems)	**L**	**T/P/D**	**C**
Elective-I	**3**	**0**	**3**

(R11 ESS 2107) ADVANCED COMPUTER ARCHITECTURE

UNIT I

Concept of instruction format and instruction set of a computer, types of operands and operations; addressing modes; processor organization, register organization and stack organization; instruction cycle; basic details of Pentium processor and power PC processor, RISC and CISC instruction set.

UNIT II

Memory devices; Semiconductor and ferrite core memory, main memory, cache memory, associative memory organization; concept of virtual memory; memory organization and mapping; partitioning, demand paging, segmentation; magnetic disk organization, introduction to magnetic tape and CDROM.

UNIT III

IO Devices, Programmed IO, interrupt driver IO, DMA IO modules, IO addressing; IO channel, IO Processor, DOT matrix printer, ink jet printer, laser printer.Advanced concepts; Horizontal and vertical instruction format, microprogramming, microinstruction sequencing and control; instruction pipeline; parallel processing; problems in parallel processing; data hazard, control hazard.

UNIT IV

ILP software approach-complier techniques-static branch protection-VLIW approach-H.W support for more ILP at compile time-H.W verses S.W solutions

Multiprocessors and thread level parallelism-symmetric shared memory architectures-distributed shared memory-Synchronization-multi threading.

UNIT V

Storage System-Types-Buses-RAID-errors and failures-bench marking a storage device designing a I/O system.

Inter connection networks and clusters-interconnection network media – practical issues in interconnecting networks-examples-clusters-designing a cluster

Text Books:

1. "Computer organization and architecture", Williams Stallings, PHI of India, 1998.
2. Computer organization, Carl Hamachar, Zvonko Vranesic and Safwat Zaky, McGraw Hill International Edition.
3. Computer Architecture & Organization, John P. Hayes, TMH III Edition.
4. Computer Architecture A quantitative approach 3rd edition John L. Hannessy & David A. Patteson Morgan Kufmann (An Imprint of Elsevier)

Reference Books:

1. "Computer Architecture and parallel Processing" Kai Hwang and A. Briggs International edition McGraw-Hill.
2. Advanced Computer Architecture, Dezso Sima, Terence Fountain, Peter Kacsuk, Pearson.

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Elective-I	**3**	**0**	**3**

(R11 ESS 2108) WIRELESS LAN'S AND PAN'S

UNIT 1: Overview of Wireless Communication

History of wireless communication, Wireless Vision, Technical Issues, Surrent Wireless Systems, The Wireless Spectrum.

Unit 2: Introduction to Wireless LANS

Historical Overview of LAN Industry, Evolution of The WLAN Industry, Wireless Home Networking, WLAN Application, WLAN Components, WLAN Modes, WLAN Standards and operation.

Unit 3: High-speed Wireless LANs and WLAN Security

IEEE 802.11a and IEEE 802.11b and other WLAN Standards, WLAN Security.

Unit 4: Low Rate Wireless Personal Area Networks

Infrared WPANs, RFWPANs, Low rate WPAN Security, High rate WPAN Standards, 802.15.3, High rate WPANs, Ultra Wideband, WPAN Challenges.
Wireless Wide Area Networks: Cellular Telephone Applications, Digital Cellular Technology, Client Software, Digital Cellular Challenges and Outlook, Satellite Broadband Wireless.
Wireless Metropolitan Area Networks: What is WMAN?, Land- Based Fixed Broadband Wireless, IEEE 802.16 (WiMAX), WMAN Security.

Unit 5: Ad-Hoc- Wireless Networks

Application, Design Principles and Challenges, Protocol Layers, Cross Layer Design, Network Capacity Limits, Energy Constrained Networks. Cellular and Adhoc wireless networks, applications, MAC protocols, Routing, Multicasting, Transport layer Protocols, quality of service browsining, deployment considerations, Adhoc wireless Internet.

TEXT BOOKS:

1. Wireless Communication- Andrea Goldsmith, Cambridge University Press.
2. Wireless Communication- Marks Ciampor, Jeorge Olenewa, 2007, Cengage Learning.
3. Wireless Networks- Kaveh Pahlaram, Prashant Krishnamurthy, 2002, PHI.

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I Year – I Sem. M.Tech. (Embedded Systems)	**L**	**T/P/D**	**C**
Elective-I	**3**	**0**	**3**

(R11 ESS 2109) ADVANCED DIGITAL SIGNAL PROCESSING

UNIT I

Review of DFT, FFT, IIR Filters, FIR Filters,

Multirate Signal Processing: Introduction, Decimation by a factor D, Interpolation by a factor I, Sampling rate conversion by a rational factor I/D, Multistage Implementation of Sampling Rate Conversion, Filter design & Implementation for sampling rate conversion, Applications of Multirate Signal Processing

UNIT II

Non-Parametric methods of Power Spectral Estimation: Estimation of spectra from finite duration observation of signals, Non-parametric Methods: Bartlett, Welch & Blackman & Tukey methods, Comparison of all Non-Parametric methods

UNIT III

Parametric Methods of Power Spectrum Estimation: Autocorrelation & Its Properties, Relation between auto correlation & model parameters, AR Models - Yule-Waker & Burg Methods, MA & ARMA models for power spectrum estimation.

UNIT –IV

Linear Prediction : Forward and Backward Linear Prediction – Forward Linear Prediction, Backward Linear Prediction, Optimum reflection coefficients for the Lattice Forward and Backward Predictors. Solution of the Normal Equations: Levinson Durbin Algorithm, Schur Algorithm. Properties of Linear Prediction Filters

UNIT V

Finite Word Length Effects: Analysis of finite word length effects in Fixed-point DSP systems – Fixed, Floating Point Arithmetic – ADC quantization noise & signal quality – Finite word length effect in IIR digital Filters – Finite word-length effects in FFT algorithms.

TEXTBOOKS:

1. Digital Signal Processing: Principles, Algorithms & Applications - J.G.Proakis & D.G.Manolokis, 4th ed., PHI.
2. Discrete Time signal processing - Alan V Oppenheim & Ronald W Schaffer, PHI.
3. DSP – A Pratical Approach – Emmanuel C.Ifeacher, Barrie. W. Jervis, 2 ed., Pearson Education.

REFERENCES:

1. Modern spectral Estimation : Theory & Application – S. M .Kay, 1988, PHI.
2. Multirate Systems and Filter Banks – P.P.Vaidyanathan – Pearson Education
3. Digital Signal Processing – S.Salivahanan, A.Vallavaraj, C.Gnanapriya, 2000,TMH

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I Year – I Sem. M.Tech. (Embedded Systems)	**L**	**T/P/D**	**C**
Elective-II	**3**	**0**	**3**

(R11VSD2107) DIGITAL SYSTEM DESIGN

Unit-I: Designing with Programmable Logic Devices

Designing with Read only memories – Programmable Logic Arrays – Programmable Array logic – Sequential Programmable Logic Devices – Design with FPGA's– Using a One-hot state assignment, State transition table- State assignment for FPGA's - Problem of Initial state assignment for One –Hot encoding - State Machine charts – Derivation of SM Charts – Realization of SM charts – Design Examples –Serial adder with Accumulator - Binary Multiplier – Signed Binary number multiplier (2's Complement multiplier) – Binary Divider – Control logic for Sequence detector – Realization with Multiplexer – PLA – PAL.

Unit-II: Fault Modeling & Test Pattern Generation

Logic Fault model – Fault detection & Redundancy- Fault equivalence and fault location –Fault dominance – Single stuck at fault model – Multiple stuck at fault models –Bridging fault model
Fault diagnosis of combinational circuits by conventional methods – Path sensitization techniques, Boolean Difference method – Kohavi algorithm – Test algorithms – D algorithm, PODEM, Random testing, Transition count testing, Signature analysis and test bridging faults.

Unit-III: Fault Diagnosis in Sequential Circuits

Circuit Test Approach, Transition Check Approach - State identification and fault detection experiment, Machine identification, Design of fault detection experiment.

Unit-IV: PLA Minimization and Testing

PLA Minimization – PLA folding, Fault model in PLA, Test generation and Testable PLA Design.

Unit-V: Minimization and Transformation of Sequential Machines

The Finite state Model – Capabilities and limitations of FSM – State equivalence and machine minimization – Simplification of incompletely specified machines.
Fundamental mode model – Flow table – State reduction – Minimal closed covers – Races, Cycles and Hazards.

TEXT BOOKS:

1. Fundamentals of Logic Design – Charles H. Roth, 5th ed., Cengage Learning.
2. Digital Systems Testing and Testable Design – Miron Abramovici, Melvin A. Breuer and Arthur D. Friedman- John Wiley & Sons Inc.
3. Logic Design Theory – N. N. Biswas, PHI

REFERENCES:

1. Switching and Finite Automata Theory – Z. Kohavi , 2nd ed., 2001, TMH
2. Digital Design – Morris Mano, M.D.Ciletti, 4th Edition, PHI.
3. Digital Circuits and Logic Design – Samuel C. Lee , PHI

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I Year – I Sem. M.Tech. (Embedded Systems)	**L**	**T/P/D**	**C**
Elective-II	**3**	**0**	**3**

(R11 ESS 2110) NEURAL NETWORKS AND APPLICATIONS

UNIT – I Fundamental Concepts, Models & Learning Rules of Artificial Neural Systems

Biological Neuron Models and their Artificial Models Biological Neuron, McCulloch-Pitts Neuron Model, Neuron Modeling for Artificial Neuron Models, Models of Artificial Neural Networks; Feed Forward Network and Feed Backward Network. Neural Processing, Supervised and Unsupervised Learning

Neural Network Learning rules: Hebbian Learning Rule, Perception Learning Rule, Delta Learning Rule Widrow-Hoff Rule, Correlation Learning Rule, Winner –Take-All Learning Rule, Out Star Learning Rule, Summary of Learning Rules.

UNIT – II Single Layer Feed Forward Networks

Classification Model, Features and Decision Regions, Discriminant Functions, Linear Machine and Minimum Distance Classification, Nonparametric Training Concept, Training and Classification using the Discrete Perceptron: Algorithm and Examples. Single Layer Continuous Perceptron Networks for Linearly Separable Classifications, Perceptron Convergence Theorem, Multicategory Single Layer Perceptron Networks.

UNIT – III Multilayer Feed Forward Networks

Linearly Nonseparable Pattern Classification, Delta Learning Rule for Multiperception layer. Generalized Delta Learning Rule. Feed Forward Recall and Error Back Propagation Training; Examples of Error Back-Propagation, Training Errors, Learning Factors; Initial weights Cumulative Weight Adjustment versus Incremental Updating, Steepness of activation function, learning constant, momentum method, Network architecture Versus Data Representation, Necessary number of Hidden Neurons. Application of Back propagation Networks in pattern recognition & Image processing

UNIT – IV Associative Memories

Basic concepts Linear associator ,Basic concepts of Dynamical systems. Mathematical Foundation of Discrete-Time Hop field Networks. Mathematical Foundation of Gradient-Type Hopfield Networks. Transient response of Continuous Time Networks. Example Solution of Optimization Problems; Summing networks with digital outputs. Minimization of the Traveling salesman tour length, Solving Simultaneous Linear Equations. Boltzman machines,Bidirectional Associative Memory; Multidirectional Associative Memory. Associative Memory of Spatio-temporal Patterns

UNIT – V Matching And Self-Organizing Networks

Hamming net and MAXNET Unsupervised learning of clusters. Clustering and similarity measures Winner take all learning ,recall mode, initialization of weights, separability limitations. Counter propagation networks. feature mapping: Self organizing feature maps. Cluster discovery networks (ART1).

TEXT BOOKS:

1. Introduction to Artificial Neural Systems - J.M.Zurada, Jaico Publishers
2. Artificial Neural Networks - Dr. B. Yagananarayana, 1999, PHI, New Delhi.

REFERENCES:

1. Elements of Artificial Neural Networks - Kishan Mehrotra, Chelkuri K. Mohan, Sanjay Ranka, Penram International
2. Artificial Neural Network –Simon Haykin, 2nd ed., Pearson Education
3. Introduction Neural Networks Using MATLAB 6.0 - S.N. Shivanandam, S. Sumati, S. N. Deepa,1/e, TMH, New Delhi.
4. Fundamental of Neural Networks –Laurene Fausett

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I Year – I Sem. M.Tech. (Embedded Systems)	**L**	**T/P/D**	**C**
Elective-II	**3**	**0**	**3**

(R11 ESS 2111) ADVANCED OPERATING SYSTEMS

Unit – I:

Introduction to Operating Systems: Overview of computer system hardware, Instruction execution, I/O function, Interrupts, Memory hierarchy, I/O Communication techniques, Operating system objectives and functions, Evaluation of operating System

Unit – II:

Introduction to UNIX and LINUX: Basic commands & command arguments, Standard input, output, Input / output redirection, filters and editors, Shells and operations

Unit – III:

System Calls: System calls and related file structures, Input / Output, Process creation & termination.
Inter process Communication: Introduction, file and record locking, Client – Server example, pipes, FIFOs, Streams & Messages, Name Spaces, Systems V IPC, Message queues, Semaphores, Shared Memory, Sockets & TLI.

Unit – IV:

Introduction to Distributed systems: Goals of distributed system, Hardware and software concepts, Design issues.
Communication in Distributed systems: Layered protocols, ATM networks, Client - Server model, Remote procedure call and Group communication.

Unit – V:

Synchronization in Distributed systems : Clock synchronization, Mutual exclusion, E-tech algorithms, Bully algorithm, Ring algorithm, Atomic transactions
Deadlocks: Dead lock in distributed systems, Distributed dead lock prevention and distributed dead lock detection.

TEXT BOOKS:

1. The design of the UNIX Operating Systems – Maurice J.Bach,1986, PHI.
2. Distributed Operating System - Andrew. S. Tanenbaum, 1994, PHI.
3. The Complete reference LINUX – Richard Peterson, 4th ed., McGraw – Hill.

REFERENCES:

1. Operating Systems : Internal and Design Principles - Stallings, 6th ed., PE.
2. Modern Operating Systems, Andrew S Tanenbaum 3rd ed., PE.
3. Operating System Principles- Abraham Silberchatz, Peter B. Galvin, Greg Gagne, 7th ed.,, John Wiley
4. UNIX User Guide – Ritchie & Yates.
5. UNIX Network Programming - W.Richard Stevens ,1998, PHI.
6. The UNIX Programming Environment – Kernighan & Pike, PE.

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I Year – I Sem. M.Tech. (Embedded Systems)	**L**	**T/P/D**	**C**
	0	**3**	**2**

(R11 VSD 2201) EMBEDDED SYSTEMS LAB-1

CYCLE 1: 8051 Microcontrollers

1. Serial Data Transmission using 8051 microcontroller in different modes.
2. Look up tables for 8051.
3. Timing subroutines for 8051- Real time times and Applications.
4. Keyboard interface to 8051.
5. ADC, DAC interface to 8051.
6. LCD interface to 8051.

CYCLE 2:

1. Study of Real Time Operating Systems.
2. Development of Devices Drivers for RT Linux.
3. Software Development for DSP Applications.
4. Serial Communication Drivers for ARM Processors.
5. Case Studies- Any two

a. Design of RTOS Kernel.
b. Cross Compiler/ Assembler.
c. Vx Works.

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I Year – II Sem. M.Tech. (Embedded Systems)	**L**	**T/P/D**	**C**
	3	**0**	**3**

(R11 ESS 2104) HARDWARE- SOFTWARE CO- DESIGN

UNIT –I

CO- DESIGN ISSUES

Co- Design Models, Architectures, Languages, A Generic Co-design Methodology.

CO- SYNTHESIS ALGORITHMS :

Hardware software synthesis algorithms: hardware – software partitioning distributed system cosynthesis.

UNIT –II

PROTOTYPING AND EMULATION:

Prototyping and emulation techniques, prototyping and emulation environments, future developments in emulation and prototyping architecture specialization techniques, system communication infrastructure

TARGET ARCHITECTURES:

Architecture Specialization techniques, System Communication infrastructure, Target Architecture and Application System classes, Architecture for control dominated systems (8051-Architectures for High performance control), Architecture for Data dominated systems (ADSP21060, TMS320C60), Mixed Systems.

UNIT – III

COMPILATION TECHNIQUES AND TOOLS FOR EMBEDDED PROCESSOR ARCHITECTURES:

Modern embedded architectures, embedded software development needs, compilation technologies practical consideration in a compiler development environment.

UNIT – IV

DESIGN SPECIFICATION AND VERIFICATION:

Design, co-design, the co-design computational model, concurrency coordinating concurrent computations, interfacing components, design verification, implementation verification, verification tools, interface verification

UNIT – V

LANGUAGES FOR SYSTEM – LEVEL SPECIFICATION AND DESIGN-I

System – level specification, design representation for system level synthesis, system level specification languages,

LANGUAGES FOR SYSTEM – LEVEL SPECIFICATION AND DESIGN-II

Heterogeneous specifications and multi language co-simulation the cosyma system and lycos system.

TEXT BOOKS :

1. Hardware / software co- design Principles and Practice – Jorgen Staunstrup, Wayne Wolf – 2009, Springer.
2. Hardware / software co- design Principles and Practice, 2002, kluwer academic publishers

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I Year – II Sem. M.Tech. (Embedded Systems)	**L**	**T/P/D**	**C**
	3	**0**	**3**

(R11 ESS 2105) DSP PROCESSORS AND ARCHITECTURES

UNIT I

INTRODUCTION TO DIGITAL SIGNAL PROCESING

Introduction, A Digital signal-processing system, The sampling process, Discrete time sequences. Discrete Fourier Transform (DFT) and Fast Fourier Transform (FFT), Linear time-invariant systems, Digital filters, Decimation and interpolation, Analysis and Design tool for DSP Systems MATLAB, DSP using MATLAB.

COMPUTATIONAL ACCURACY IN DSP IMPLEMENTATIONS

Number formats for signals and coefficients in DSP systems, Dynamic Range and Precision, Sources of error in DSP implementations, A/D Conversion errors, DSP Computational errors, D/A Conversion Errors, Compensating filter.

UNIT II

ARCHITECTURES FOR PROGRAMMABLE DSP DEVICES

Basic Architectural features, DSP Computational Building Blocks, Bus Architecture and Memory, Data Addressing Capabilities, Address Generation Unit, Programmability and Program Execution, Speed Issues,Features for External interfacing.

UNIT III

EXECUTION CONTROL AND PIPELINING

Hardware looping, Interrupts, Stacks, Relative Branch support, Pipelining and Performance, Pipeline Depth, Interlocking, Branching effects, Interrupt effects, Pipeline Programming models.

PROGRAMMABLE DIGITAL SIGNAL PROCESSORS

Commercial Digital signal-processing Devices,Data Addressing modes of TMS320C54XX DSPs, Data Addressing modes of TMS320C54XX Processors, Memory space of TMS320C54XX Processors, Program Control, TMS320C54XX instructions and Programming, On-Chip Peripherals, Interrupts of TMS320C54XX processors, Pipeline operation of TMS320C54XX Processors.

UNIT IV

IMPLEMENTATIONS OF BASIC DSP ALGORITHMS

The Q-notation, FIR Filters, IIR Filters, Interpolation Filters, Decimation Filters, PID Controller, Adaptive Filters, 2-D Signal Processing.

IMPLEMENTATION OF FFT ALGORITHMS

An FFT Algorithm for DFT Computation, A Butterfly Computation, Overflow and scaling, Bit-Reversed index generation, An 8-Point FFT implementation on the TMS320C54XX, Computation of the signal spectrum.

UNIT V

INTERFACING MEMORY AND I/O PERIPHERALS TO PROGRAMMABLE DSP DEVICES

Memory space organization, External bus interfacing signals, Memory interface, Parallel I/O interface, Programmed I/O, Interrupts and I/O, Direct memory access (DMA).

A Multichannel buffered serial port (McBSP), McBSP Programming, a CODEC interface circuit, CODEC programming, A CODEC-DSP interface example.

TEXT BOOKS

1. Digital Signal Processing – Avtar Singh and S. Srinivasan, Thomson Publications, 2004.
2. DSP Processor Fundamentals, Architectures & Features – Lapsley et al. S. Chand & Co, 2000.

REFERENCES

1. Digital Signal Processors, Architecture, Programming and Applications – B. Venkata Ramani and M. Bhaskar, TMH, 2004.
2. Digital Signal Processing – Jonatham Stein, John Wiley, 2005.

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I Year – II Sem. M.Tech. (Embedded Systems)	**L**	**T/P/D**	**C**
	3	**0**	**3**

(R11 ESS 2106) SYSTEM MODELING & SIMULATION

UNIT I

Basic Simulation Modeling, Systems, Models and Simulation, Discrete Event Simulation, Simulation of single server queing system, Characterizing Systems, Simulation Diagrams.

UNIT II: Stochastic generators

Uniformly Distributed Random Numbers, Statistical properties of [0,1] generators, Generation of Non-uniform and Arbitary Random variates, Random processes,Characterizing and generating random process, White Noise.

MODELING TIME DRIVEN SYSTEMS: Modeling input signals, delays, System integration, Linear Systems, Motion control models, Numerical Experimentation.

EXOGENOUS SIGNALS AND EVENTS: Disturbance signals, State Machines, Petri Nets & Analysis, System encapsulation.

UNIT III : MARKOV PROCESS

Probabilistic systems, Discrete Time Markov processes, Random walks, Poisson processes, the exponential distribution, simulating a poison process, Continuous-Time Markov processes.

EVENT DRIVEN MODELS: Simulation diagrams, Queing theory, simulating queing systems, Finite Capacity Queues, Multiple Servers,M/M/C Queues.

UNIT IV : SYSTEM OPTIMIZATION

System Identification, Searches, Alpha/beta trackers, Multidimensional Optimization, Modeling and Simulation methodology.

UNIT V : SIMULATION SOFTWARE and Building Simulation Models

Comparison of simulation packages with Programming languages, Classification of Software, Desirable Software features, General purpose simulation packages – Arena, Extend Guidelines for determining levels of model detail, Techniques for increasing model validity and credibility.

TEXTBOOKS

1.System Modeling & Simulation, An Introduction – Frank L. Severance, John Wiley & Sons, 2001.
2.Simulation Modelling and Analysis – Averill M. Law, W. David Kelton, TMH, 3rd Edition, 2003.

REFRENCE BOOKS

1.Systems Simulation – Geoffery Gordon, PHI, 1978.

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I Year – II Sem. M.Tech. (Embedded Systems)	**L**	**T/P/D**	**C**
	3	**0**	**3**

(R11 ESS 2101) CPLD AND FPGA ARCHITECTURE AND APPLICATIONS

UNIT –I

Programmable logic : ROM, PLA, PAL PLD, PGA – Features, programming and applications using complex programmable logic devices Altera series – Max 5000/7000 series and Altera FLEX logic-10000 series CPLD, AMD's- CPLD (Mach 1to 5), Cypres FLASH 370 Device technology, Lattice PLST's architectures – 3000 series – Speed performance and in system programmability.

UNIT – II

FPGAs: Field Programmable gate arrays- Logic blocks, routing architecture, design flow technology mapping j for FPGAs, Case studies Xitir x XC4000 & ALTERA's FLEX 8000/10000 FPGAs: AT &T ORCA's (Optimized Reconfigurable Cell Array): ACTEL's ACT-1,2,3 and their speed performance

UNIT-III

Alternative realization for state machine chat suing microprogramming linked state machine one – hot state machine, petrinetes for state machines-basic concepts, properties, extended petrinetes for parallel controllers.

UNIT-IV

Digital front end digital design tools for FPGAs& ASICs: Using mentor graphics EDA tool ("FPGA Advantage") – Design flow using FPGAs.

UNIT - V

Case studies of paraller adder cell paraller adder sequential circuits, counters, multiplexers, parallel controllers.

TEXT BOOKS:

1. Field Programmable Gate Array Technology - S. Trimberger, Edr, 1994, Kluwer Academic Publications.
2. Field Programmable Gate Arrays, John V.Oldfield, Richard C Dore, Wiley Publications.

REFERENCES :

1. Digital Design Using Field Programmable Gate Array, P.K.Chan & S. Mourad, 1994, Prentice Hall.
2. Digital System Design using Programmable Logic Devices – Parag.K.Lala, 2003, BSP.
3. Field programmable gate array, S. Brown, R.J.Francis, J.Rose ,Z.G.Vranesic, 2007, BSP.
4. Digital Systems Design with FPGA's and CPLDs – Ian Grout, 2009, Elsevier.

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I Year – II Sem. M.Tech. (Embedded Systems)	**L**	**T/P/D**	**C**
Elective- III	**3**	**0**	**3**

(R11 VSD 2112) LOW POWER VLSI DESIGN

UNIT I

LOW POWER DESIGN, AN OVER VIEW: Introduction to low- voltage low power design, limitations, Silicon-on-Insulator.

MOS/BiCMOS PROCESSES : Bi CMOS processes, Integration and Isolation considerations, Integrated Analog/Digital CMOS Process.

UNIT II

LOW-VOLTAGE/LOW POWER CMOS/ BICMOS PROCESSES: Deep submicron processes ,SOI CMOS, lateral BJT on SOI, future trends and directions of CMOS/BiCMOS processes.

UNIT III

DEVICE BEHAVIOR AND MODELING: Advanced MOSFET models, limitations of MOSFET models,Bipolar models.

Analytical and Experimental characterization of sub-half micron MOS devices, MOSFET in a Hybrid-mode environment.

UNIT IV

CMOS AND Bi-CMOS LOGIC GATES: Conventional CMOS and BiCMOS logic gates. Performance evaluation

LOW-VOLTAGE LOW POWER LOGIC CIRCUITS: Comparison of advanced BiCMOS Digital circuits. ESD-free Bi CMOS , Digital circuit operation and comparative Evaluation.

UNIT V

LOW POWER LATCHES AND FLIP FLOPS: Evolution of Latches and Flip flops-quality measures for latches and Flip-flops, Design perspective.

TEXT BOOK:

1. CMOS/BiCMOS ULSI low voltage, low power by Yeo Rofail/ Gohl(3 Authors)- Pearson Education Asia 1st Indian reprint,2002

REFERENCES:

1. Digital Integrated circuits , J.Rabaey PH. N.J 1996
2. CMOS Digital ICs sung-moKang and yusuf leblebici 3rd edition TMH 2003 (chapter 11)
3. VLSI DSP systems , Parhi, John Wiley & sons, 2003 (chapter 17)
4. IEEE Trans Electron Devices, IEEE J.Solid State Circuits, and other National and International Conferences and Symposia.

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I Year – II Sem. M.Tech. (Embedded Systems)	**L**	**T/P/D**	**C**
Elective- III	**3**	**0**	**3**

(R11 ESS 2112) ROBOTICS

UNIT-1: Introduction & Basic Definitions

Introduction, control programs for Robots, Industry Applications of Robots, Pick and Place, Gantry and Arm type Robots in typical set-ups like automobile Industry

Coordinate Systems: Cartesian, Cylindrical, Polar and revolute systems: Robot Positioning: Robot Arms: Axes, their ranges, offset and In-line wrist: Roll, Pitch and Yaw, their meaning in Robotics

UNIT-II : Mechanical Aspects

Kinematics, Inverse Kinematics, Motion planning and Mobile Mechanisms.

UNIT-III: Sensors and Applications

Range and Use of Sensor, Micro switches, Resistance Transducers, Piezo-electric, Infrared and Lasers, Applications of sensors: Reed Switches, Ultrasonic, Barcode Readers and RFID

UNIT-IV: Robot Systems

Hydraulic and Electrical Systems including pumps, valves, solenoids, cylinders, stepper motors, Encoders and AC Motors

UNIT – V: Programming of Robots

Programming of Robots such as Lego Robots, Programming environment, Example Applications, Safety considerations

TEXT BOOKS:

1. Introduction to Robotics – P.J.Mckerrow,ISBN:0201182408
2. Introduction to Robotics – S.Nikv,2001,Prentice Hall,
3. Mechatronics and Robotics: Design & Applications – A.Mutanbara,1999,CRC Press.

REFERENCE BOOK

1. Robotics – K.S.Fu, R.C.Gonzalez and C.S.G.Lee,2008,TMH.

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I Year – II Sem. M.Tech. (Embedded Systems)	**L**	**T/P/D**	**C**
Elective- III	**3**	**0**	**3**

(R11 ESS 2113) ADHOC WIRELESS AND SENSOR NETWORKS

UNIT-I :

Wireless LANS and PANS : Introduction, Fundamentals of WLANS, IEEE 802.11 Standard, HIPERLAN standard, Bluetooth, Home RF.

Wireless Internet: Wireless Internet, Mobile IP,TCP in wireless domain, WAP,Optimizing Web over Wireless.

UNIT II

ADHOC Wireless Networks : Introduction, Issues in Ad Hoc wireless networks, AD Hoc wireless Internet.

MAC Protocols for Ad Hoc Wireless Networks: Introduction, in designing a MAC protocol for Ad Hoc wireless networks, Design goals of MAC protocol for AdHoc wireless network, classification of MAC Protocols, Contention-based protocols with scheduling mechanisms, MAC protocols that use directional antenns, other MAC protocols.

UNIT III

ROUTINGPROTOCOLS:

Introduction – Issues in Designing a Routing Protocol for Ad Hoc Wireless Networks – Classifications of Routing Protocols – Table–Driven Routing Protocols ,On–Demand Routing protocols, Hybrid routing protocols, Routing protocols with efficient flooding mechanisms, Hierachical routing protocols, power-aware routing protocols.

TRANSPORT LAYER– SECURITY PROTOCOLS

Introduction – Issues in Designing a Transport Layer Protocol for Ad hoc Wireless Networks – Design Goals of a Transport Layer Protocol for Ad hoc Wireless Networks –Classification of Transport Layer Solutions – TCP over Ad hoc Wireless Networks – Other Transport Layer Protocols for Ad hoc Wireless Networks – Security in Ad Hoc Wireless Networks – Network Security Requirements – Issues and Challenges in Security Provisioning – Network Security Attacks – Key Management – Secure Routing in Ad hoc Wireless Networks.

UNIT IV

Quality of Service

Introduction – Issues and Challenges in Providing QoS in Ad hoc Wireless Networks –Classifications of QoS Solutions – MAC Layer Solutions – Network Layer Solutions – QoS Frameworks for Ad hoc Wireless Networks

Energy Management in Ad hoc Wireless Networks

Introduction – Need for Energy Management in Ad hoc Wireless Networks – Classification of Adhoc Wireless Networks – Battery Management Schemes – Transmission Power Management Schemes – System Power Management Schemes.

UNIT V

WIRELESS SENSOR NETWORKS

Introduction, Sensor Network Architecture, Data Dissemination, Data Gathering, MAC protocols for Sensor Networks, Location discovery, Quality of Sensor network, Evolving standards, Other issues

TEXTBOOK:

1. C. Siva Ram Murthy and B. S. Manoj, “Ad Hoc Wireless Networks Architectures and Protocols”, Prentice Hall, PTR, 2004.
2. Wireless Adhoc and Sensor Networks: Protocols, Performance and control – Jagannathan Sarangapani, CRC Press

REFERENCES:

1. C. K. Toh, “Ad Hoc Mobile Wireless Networks Protocols and Systems”, Pearson Education
2. Wireless Sensor Networks – C.S. Raghavendra, Krishna M. Sivalingam, 2004, Springer

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I Year – II Sem. M.Tech. (Embedded Systems)	**L**	**T/P/D**	**C**
Elective- IV	**3**	**0**	**3**

(R11 VSD 2110) IMAGE AND VIDEO PROCESSING

UNIT 1

Fundamentals steps of Image processing and Image transforms

Basic steps of image processing system sampling and quantization of an image – basic relationship between pixels.

Image transforms: 2D-Discrete Fourier Transform, Discrete Cosine transform(DCT), Wavelet Transform: Continous Wavelet Transforms, Discrete Wavelet Transforms

UNIT 2 : Image Processing Techniques

Image Enhancement

Spatial Domain methods: Histogram Processing, Fundamentals of spatial filtering, Smoothing spatial filters, Sharpening spatial filters

Frequency domain methods: Basics of filtering in frequency domain, image smoothing, image sharpening, selective filtering.

Image Segmentation

Segmentation concepts, Point, Line and Edge detection, Thresholding, Region based segmentation

UNIT 3: Image Compression

Image Compression Fundamentals – Coding Redundancy, Spatial and Temporal Redundancy, Compression models: Lossy & Lossless, Huffman coding, Arithmetic coding, LZW coding, Run Length coding, Bit plane coding, Transform coding, Predictive coding, wavelet coding, JPEG standards.

UNIT 4 Basic Steps of video processing

Analog video, Digital video. Time- varying Image Formation models: Three – dimensional motion models, Geometric Image Formation, Photometric Image Formation, Sampling of video signals, Filtering operations.

UNIT 5

2-D motion estimation: Optical flow, General methodologies, Pixel based motion estimation, Block matching algorithm, Mesh-based motion estimation , Global motion estimation, Region based motion estimation, Multiresolution motion estimation, Waveform based coding, Block based transform coding, Predictive coding. Application of motion estimation in video coding

TEXT BOOKS

1. Digital Image processing – Gonzaleze and woods,3rd ed., Pearson
2. Video processing and communication – Yao Wang, Joern Ostermann and Ya-Qin Zhang, I Ed Prentice Hall

REFERENCE BOOKS

1. Digital video processing – M. Tekalp, Prentice Hall International

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I Year – II Sem. M.Tech. (Embedded Systems)	**L**	**T/P/D**	**C**
Elective- IV	**3**	**0**	**3**

(R11 VSD 2104) SYSTEM ON CHIP ARCHITECTURE

UNIT-1:

Introduction to Processor Design: Abstraction in Hardware Design, MUO a simple processor, processor design trade off, Design for low power consumption.

ARM Processor as System –on-Chip: Acron RISC Machine-Architecture inherence-Arm Programming model-ARM development tools-3 and 5 stage pipeline ARM organization - ARM Instruction execution and implementation -ARM Co-Processor interface.

UNIT-2:

ARM Assembly Language Programming: ARM instruction types -Data transfer, data processing and control flow instructions -ARM Instruction set-Co-processor instructions.

Architecture support for High Level Language: Data types-abstraction in software design- Expressions –Loops-Functions and procedures-Conditional Statements-Use of Memory.

UNIT-3:

Memory Hierarchy: Memory size and speed-On-Chip memory-Caches-Cache design-an example-memory management.

UNIT-4:

Architectural Support for System Development: Advanced Microcontroller Bus architecture (AMBA)-ARM memory interface-ARM reference peripheral specification – Hardware system Prototyping Tools –Armulator-Debug architecture.

UNIT-5:

Architectural Support for Operating Systems: An introduction to Operating Systems - ARM system control co processor -CP15 Protection unit registers -ARM Protection unit-CP15 MMU registers-ARM MMU Architecture-Synchronization-Context Switching input and output.

TEXT BOOKS:

1. ARM System on Chip Architecture –Steve Furber-2nd ed., 2000, Addison Wesley Professional.
2. Design of System on a Chip: Devices and C omponents-Ricardo Reis, 1st ed., 2004, Springer

REFERENCES:

1. Co-Verification of Hardware and Software for ARM System on Chip Design (Embedded Technology)-Jason Andrews—Newnes, BK and CDROM
2. System on Chip Verification –Methodologies and Techniques -Prakash Rashinkar, Peter Paterson and Leena Sing L, 2001, Kluwer Academic Publishers

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I Year – II Sem. M.Tech. (Embedded Systems)	**L**	**T/P/D**	**C**
Elective- IV	**3**	**0**	**3**

(R11 ESS 2114) NETWORK SECURITY AND CRYPTOGRAPHY

UNIT-I

Introduction:

Attacks, Services and Mechanisms, Security attacks, Security services, A Model for Internetwork security.Classical Techniques: Conventional Encryption model, Steganography, Classical Encryption Techniques.

UNIT-II

Modern Techniques:

Simplified DES, Block Cipher Principles, Data Encryption standard, Strength of DES, Differential and Linear Cryptanalysis, Block Cipher Design Principles and Modes of operations.

Algorithms: Triple DES, International Data Encryption algorithm, Blowfish, RC5, CAST-128, RC2, Characteristics of Advanced Symmetric block cifers.

Conventional Encryption: Placement of Encryption function, Traffic confidentiality, Key distribution, Random Number Generation.

Public Key Cryptography: Principles, RSA Algorithm, Key Management, Diffie-Hellman Key exchange, Elliptic Curve Cryptography.

UNIT-III

Number theory

Prime and Relatively prime numbers, Modular arithmetic, Fermat's and Euler's theorems, Testing for primality, Euclid's Algorithm, the Chinese remainder theorem, Discrete logarithms.

Message authentication and Hash functions:

Authentication requirements and functions, Message Authentication, Hash functions, Security of Hash functions and MACs.

UNIT-IV

Hash and Mac Algorithms

MD File, Message digest Algorithm, Secure Hash Algorithm, RIPEMD-160, HMAC. Digital signatures and Authentication protocols:

Digital signatures, Authentication Protocols, Digital signature standards.

Authentication Applications:

Kerberos, X.509 directory Authentication service.Electronic Mail Security: Pretty Good Privacy, S/MIME.

UNIT-V

IP Security

Overview, Architecture, Authentication, Encapsulating Security Payload, Combining security Associations, Key Management.

Web Security

Web Security requirements, Secure sockets layer and Transport layer security, Secure Electronic Transaction.

Intruders, Viruses and Worms : Intruders, Viruses and Related threats.

Fire Walls : Fire wall Design Principles, Trusted systems.

TEXT BOOKS:

1. Cryptography and Network Security: Principles and Practice - William Stallings, 2000, PE.

REFERENCES:

1. Principles of Network and Systems Administration, Mark Burgess,John Wiel

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I Year – II Sem. M.Tech. (Embedded Systems)	**L**	**T/P/D**	**C**
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(R11 ESS 2202) EMBEDDED SYSTEMS LAB-II Using PS0C

1. Understanding the overall programming Environment of PSOC and using PSOC First Touch kit
2. Addressing/Control of on-board resources using the first touch kit
3. Study and characterization of the Programmable gain Amplifier (PGA): Gain Bandwidth product.
4. Realization of Low-pass, High-pass and Band-pass filters and their characterization
5. Experiments with on-chip ADC's and DAC's
6. Digital Function Implementation using Digital blocks.
7. Logical/Arithmetic function implementation using Microcontroller
8. Timer operation in different Modes
9. Interrupt control
10. I/O Operations: Input from keyboard and display of numerals and strings
11. Implementation of Serial communications
12. Applications

    i. LED control and Pattern generation
    ii. Stepper Motor control