A18

M.Tech. (VLSI SYSTEM DESIGN)

M.Tech. Amended R18 [A18] CBCS Curriculum

VNR VIGNANA JYOTHI INSTITUTE OF ENGINEERING AND TECHNOLOGY

An Autonomous, ISO 9001:2015 & QS I-Gauge Diamond Rated Institute, Accredited by NAAC with 'A++' Grade
NBA Accreditation for B.Tech. CE, EEE, ME, ECE, CSE, EIE, IT Programmes
Approved by AICTE, New Delhi, Affiliated to JNTUH, NIRF 135th Rank in Engineering Category
Recognized as "College with Potential for Excellence" by UGC
Vignana Jyothi Nagar, Pragathi Nagar, Nizampet (S.O), Hyderabad – 500 090, TS, India.
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VISION OF THE INSTITUTE

To be a World Class University providing value-based education, conducting interdisciplinary research in cutting edge technologies leading to sustainable development of the nation

MISSION OF THE INSTITUTE

- To produce technically competent and socially responsible engineers, managers and entrepreneurs, who will be future ready.

- To involve students and faculty in innovative research projects linked with industry, academic and research institutions in India and abroad.

- To use modern pedagogy for improving the teaching-learning process.

DEPARTMENT OF

ELECTRONICS AND COMMUNICATION ENGINEERING

VISION OF THE DEPARTMENT

A resource centre of academic excellence for imparting technical education with high pattern of discipline through dedicated staff which shall set global standards, making National and International students technologically superior and ethically strong, who in turn shall improve the quality of life.

MISSION OF THE DEPARTMENT

- To provide quality education in the domain of Electronics and Communication Engineering through effective learner centric process.
- To provide industry specific best of breed laboratory facilities beyond curriculum to promote diverse collaborative research for meeting the changing industrial and societal needs.

M.TECH.
(VLSI SYSTEM DESIGN)

M.TECH. (VLSI SYSTEM DESIGN)

PROGRAM EDUCATIONAL OBJECTIVES

PEO-I: Identify, formulate and analyze technical problems in areas like semiconductor technologies, VLSI Signal verification and Design verification and testing.

PEO-II: Design and implementation of VLSI architectures using FPGA.

PEO-III: Use the techniques, skills, modern Electronic Design Automation (EDA) tools to evaluate and analyze the performance of the systems in VLSI domain.

M.TECH. (VLSI SYSTEM DESIGN)

PROGRAM OUTCOMES

PO-1: Apply acquired knowledge from undergraduate engineering and other disciplines to identify, formulate and present solutions to technical problems related to various areas of VLSI.

PO-2: Learn advanced technologies and analyze complex problems in the fields of VLSI.

PO-3: Design and implementation of VLSI architectures using FPGA/CPLD.

PO-4: Addressing specific problems in the field of VLSI system design in the form of mini projects, analysis and interpretation of data and synthesis of information to provide valid conclusions.

PO-5: Use the techniques, skills, modern Electronic Design Automation (EDA) tools, software and equipment necessary to evaluate and analyze the systems in VLSI design environments.

PO-6: Understand and commit to professional ethics, social responsibilities and norms of engineering practice.

PO-7: Develop confidence for self-education and imbibe professional values for lifelong learning.

PO-8: Demonstrate effective oral and written communication skills in accordance with technical standards.

PO-9: Become knowledgeable about contemporary developments.

PO-10: Ability to correct the mistakes effectively and learn from them to become good leaders.

PO-11: Understand the scenario of global business.

VNR VIGNANA JYOTHI INSTITUTE OF ENGINEERING AND TECHNOLOGY, HYDERABAD
M.TECH. I YEAR COURSE STRUCTURE AND SYLLABUS

(VLSI SYSTEM DESIGN)

I SEMESTER **A18**

Course Type	Course Code	Name of the Course	L	T	P	Credits
Professional Core-I	A18PC1VS01	Simulation and Synthesis with PLDs	3	0	0	3
Professional Core-II	A18PC1VS02	Digital IC Design	3	0	0	3
Professional Core-III	A18PC1VS03	Analog IC Design	3	0	0	3
Professional Elective-I	A18PE1ES02	Internet of Things	3	0	0	3
	A18PE1VS01	Full Custom IC Design				
	A18PE1VS02	VLSI Process Technology				
Professional Elective-II	A18PE1ES04	Parallel Processing	3	0	0	3
	A18PE1VS03	Advanced Digital Signal Processing				
	A18PE1VS04	Semiconductor Device Modeling				
Professional Core Lab-I	A18PC2VS01	Simulation and Synthesis with PLDs Laboratory	0	0	3	1.5
Professional Core Lab-II	A18PC2VS02	IC Design Laboratory	0	0	3	1.5
Project	A18PW4VS01	Technical Seminar	0	0	4	2
Audit	A18AU5CS01	Research Methodology and IPR	2	0	0	0
Total			**17**	**0**	**10**	**20**

VNR VIGNANA JYOTHI INSTITUTE OF ENGINEERING AND TECHNOLOGY, HYDERABAD
M.TECH. I YEAR COURSE STRUCTURE AND SYLLABUS

(VLSI SYSTEM DESIGN)

II SEMESTER **A18**

Course Type	Course Code	Name of the Course	L	T	P	Credits
Professional Core-IV	A18PC1VS04	Mixed Signal and RF IC Design	3	0	0	3
Professional Core-V	A18PC1VS05	VLSI Design for Verification and Testing	3	0	0	3
Professional Core-VI	A18PC1VS06	Low Power VLSI Design	3	0	0	3
Professional Elective-III	A18PE1ES06	SOC and NOC Architectures	3	0	0	3
	A18PE1VS05	Optimization Techniques in VLSI Design				
	A18PE1VS06	Scripting Languages for VLSI				
Professional Elective-IV	A18PE1VS07	Physical Design Automation	3	0	0	3
	A18PE1VS08	Image and Video Processing				
	A18PE1VS09	Memory Technologies				
Professional Core Lab-III	A18PC2VS03	Mixed Signal and RF IC Design Laboratory	0	0	3	1.5
Professional Core Lab-IV	A18PC2VS04	VLSI Design Verification and Testing Laboratory	0	0	3	1.5
Project	A18PW4VS02	Mini-Project	0	0	4	2
Audit	A18AU5EN01	English for Academic and Research Writing	2	0	0	0
Total			**17**	**0**	**10**	**20**

VNR VIGNANA JYOTHI INSTITUTE OF ENGINEERING AND TECHNOLOGY, HYDERABAD
M.TECH. II YEAR COURSE STRUCTURE AND SYLLABUS

(VLSI SYSTEM DESIGN)

III SEMESTER **A18**

Course Type	Course Code	Name of the Course	L	T	P	Credits
Professional Elective-V	A18OE1MT01	Selected Topics in Mathematics	3	0	0	3
	A18PE1VS10	VLSI Signal Processing				
	A18PE1VS11	Nanomaterials and Nanotechnology				
Open Elective	A18OE1CN01	Business Analytics	3	0	0	3
	A18OE1AM01	Industrial Safety				
	A18OE1AM02	Operations Research				
	A18OE1AM03	Composite Materials				
	A18OE1PS01	Waste to Energy				
Project	A18PW4VS03	Project Part - I	0	0	16	8
Total			**6**	**0**	**16**	**14**

IV SEMESTER **A18**

Course Type	Course Code	Name of the Course	L	T	P	Credits
Project	A18PW4VS04	Project Part - II	0	0	28	14
Total			**0**	**0**	**28**	**14**

VNR VIGNANA JYOTHI INSTITUTE OF ENGINEERING AND TECHNOLOGY

M.Tech. I Semester (VLSI)	**L**	**T/P**	**C**
	3	**0**	**3**

(A18PC1VS01) SIMULATION AND SYNTHESIS WITH PLDs

COURSE PRE-REQUISITES: Basic Concepts of Digital Systems

COURSE OBJECTIVES:
- To introduce Verilog HDL for the design and functionality verification of a digital circuit
- To understand the design of data path and control circuits for sequential machines
- To introduce the concept of realizing a digital circuit using PLDs

COURSE OUTCOMES: After completion of the course, students should be able to
CO-1: Develop the Verilog HDL to design a digital circuit
CO-2: Appreciate the analysis of finite state machine of a controlling circuit
CO-3: Understand the Static Timing Analysis and clock issues in digital circuits
CO-4: Verify the functionality of the digital designs using PLDs

UNIT-I:
Verilog HDL: Importance of HDLs, Lexical Conventions of Verilog HDL
Gate Level Modeling: Built in primitive gates, switches, gate delays
Data Flow Modeling: Continuous and implicit continuous assignment, delays
Behavioral Modeling: Procedural constructs, Control and repetition Statements, delays, function and tasks.

UNIT-II:
Digital Design: Design of BCD Adder, State graphs for control circuits, shift and add multiplier, Binary divider.
FSM and SM Charts: Finite state diagram, Implementation of sequence detector using FSM, State machine charts, Derivation of SM Charts, Realization of SM Chart, Implementation of Binary Multiplier.

UNIT-III:
ASIC Design Flow: Simulation, simulation types, Synthesis, synthesis methodologies, translation, mapping, optimization, Floor planning, Placement, routing, Clock tree synthesis, Physical verification.

UNIT-IV:
Static Timing Analysis: Timing paths, Meta-stability, Clock issues, Need and design strategies for multi-clock domain designs, setup and hold time Violations, steps to remove Setup and hold time violations.

UNIT-V:
Digital Design using PLD's: ROM, PLA, PAL- Registered PAL's, Configurable PAL's, GAL. CPLDs: Features, programming and applications using complex programmable logic devices, Altera Max - 7000 series and Altera FLEX logic- 10000 series CPLD.

UNIT-VI:
FPGAs: Field Programmable gate arrays Logic blocks, routing architecture, design flow, technology mapping for FPGAs, Spartan3E, Spartan XC6SLX45, Spartan 6 LX45 FPGA, Zynq-7000, Architectures and their speed performance.

TEXT BOOKS:
1. Verilog HDL, A Guide to Digital Design and Synthesis, Samir Palnitkar, 2nd Edition, 2003
2. Fundamentals of Logic Design, Charles H. Roth, 5th Edition, Cengage Learning, 2010

3. Verilog HDL Synthesis-A Practical Primer, Bhasker J., 1st Edition, 1998

REFERENCES:

1. Modern Digital Electronics, P. Jain, 3rd Edition, TMH, 2003
2. Data Sheets for CPLD & FPGA Architectures, 1996
3. Digital Principles and Design, Donald D. Givone TMH, 2016
4. Designing with FPGAs & CPLDs, Bob Zeidman, CMP Books, 2002
5. Modern Digital Design, Richard S. Sandige, MGH International Edition, 1990

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M.Tech. I Semester (VLSI)	**L**	**T/P**	**C**
	3	**0**	**3**

(A18PC1VS02) DIGITAL IC DESIGN

COURSE PRE-REQUISITES: Concepts on MOSFETS, Digital Electronic Circuits, VLSI Design

COURSE OBJECTIVES:
- To learn various design styles for combinational Circuits
- To understand the issues in CMOS digital design
- To design different high performance and low area VLSI circuits
- To discuss the VLSI memory architectures

COURSE OUTCOMES: After completion of the course, students should be able to
CO-1: Create models of digital circuits using various design styles
CO-2: Design static CMOS circuits at the transistor level
CO-3: Analyze high performance VLSI circuits
CO-4: Understand the concepts various memory elements

UNIT-I:
Introduction to MOS Device: MOS Transistor-First Glance at the MOS device, MOS Transistor under static conditions, threshold voltage, Resistive operation, saturation region, channel length modulation, velocity saturation, hot carrier effect, subthreshold conduction.
Pseudo NMOS Logic: Inverter, Inverter threshold voltage, Output high voltage, Output Low voltage, Gain at gate threshold voltage, Pseudo NMOS logic gates.

UNIT-II:
CMOS Inverter: Introduction, The static CMOS Inverter An intuitive Perspective, Static and Dynamic behaviors of CMOS Inverter, Power, Energy and Energy-delay, Technology scaling and its impact on the Inverter metrics.

UNIT-III:
Combinational MOS Logic Circuits: MOS logic circuits with NMOS loads, Static CMOS design, CMOS static properties, A complementary CMOS design, Primitive CMOS logic gates –NOR & NAND gate, Complex Logic circuits design, Realizing Boolean expressions using NMOS gates and CMOS gates, AOI and OIA designs, CMOS full adder, pass transistor logic, Differential pass transistor logic, CMOS transmission gates and design.

UNIT-IV:
Dynamic Logic Circuits: Basic principle, Voltage Bootstrapping, Synchronous dynamic pass transistor circuits, Dynamic CMOS transmission gate logic, High performance Dynamic CMOS circuits.

UNIT-V:
Sequential MOS Logic Circuits: Behavior of bi-stable elements, SR Latch, Clocked latch and flip flop circuits, CMOS D- latch and edge triggered flip flops.

UNIT-VI:
Semiconductor Memories: Types, RAM array organization, DRAM Types, Operation, Leakage currents in DRAM cell and refresh operation, SRAM operation Leakage currents in SRAM cells, Flash Memory- NOR flash and NAND flash.

TEXT BOOKS:
1. Digital Integrated Circuits–A Design Perspective, Jan M. Rabaey, Anantha Chandrakasan, Borivoje Nikolic, 2nd Ed., PHI, 2002

2. Digital Integrated Circuit Design, Ken Martin, Oxford University Press, 2011
3. CMOS Digital Integrated Circuits Analysis and Design, Sung-Mo Kang, Yusuf Leblebici, TMH, 3rd Ed., 2011

REFERENCES:

1. Introduction to VLSI Systems: A Logic, Circuit and System Perspective, Ming-BO Lin, CRC Press, 2011
2. Principles of CMOS VLSI Design, Neil H. E. Weste and Kamran Eshraghian, 2nd Edition, Addition Wesley, 1998

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M.Tech. I Semester (VLSI)	**L**	**T/P**	**C**
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(A18PC1VS03) ANALOG IC DESIGN

COURSE PRE-REQUISITES: Knowledge of MOSFET and BJT Device Models

COURSE OBJECTIVES:
- To learn the device physics of CMOS
- To know design of single stage amplifier
- To study differential amplifiers and analog CMOS sub circuits
- To discuss the design of feedback and CMOS Operational Amplifiers

COURSE OUTCOMES: After completion of the course, students should be able to
CO-1: Analyze how the simplified device models can be developed
CO-2: Able to design single stage amplifiers
CO-3: Design current mirrors, differential amplifiers
CO-4: Understand the concepts of advanced operational amplifiers

UNIT-I:
Basic MOS Device Physics: General considerations, MOS I/V Characteristics, second order Effects, MOS Device Models

UNIT-II:
CMOS Single Stage Amplifiers: Common source amplifier with different loads, source follower, Common gate amplifier, Cascode Amplifiers,
Frequency Response of Integrated circuits: frequency response (miller effect) of CG, CS, CD,

UNIT-III:
Analog CMOS Sub-Circuits: Passive & Active Current Mirrors, Basic current mirrors, Cascode current mirror, Active loads, voltage and current references.

UNIT-IV:
Differential Amplifiers: Single ended Differential operation, Basic differential pair, common Mode Response, Differential pair with MOS Loads, Frequency response of Cascade & Differential Pair with MOS Loads.

UNIT-V:
Feedback: Ideal feedback equation, gain sensitivity, feedback configurations, practical Configuration and effect of loading, Effect of Feedback on Noise.

UNIT-VI:
CMOS Operational Amplifiers: Design of CMOS Op Amps, Compensation of Op Amps, Design of Two-Stage Op Amps, Power- Supply Rejection Ratio of Two-Stage Op Amps, Cascode Op Amps.

TEXT BOOKS:
1. Design of Analog CMOS Integrated Circuits, Behzad Razavi, TMH Edition, 2012
2. CMOS Analog Circuit Design, Philip E. Allen and Douglas R. Holberg, Oxford University Press, International Second Edition/Indian Edition, 2010
3. Analysis and Design of Analog Integrated Circuits, Paul R. Gray, Paul J. Hurst, S. Lewis and R. G. Meyer, Wiley India, Fifth Edition, 2010

REFERENCES:
1. Analog Integrated Circuit Design, David A. Johns, Ken Martin, Wiley Student Ed., 2013

2. CMOS: Circuit Design, Layout and Simulation, Baker, Li and Boyce, PHI, 2012

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M.Tech. I Semester (VLSI)	**L**	**T/P**	**C**
	3	**0**	**3**

(A18PE1ES02) INTERNET OF THINGS

COURSE PRE-REQUISITES: Concepts of Programming in Java, C/C++, Embedded C, Concepts of Wireless Communication and Networking

COURSE OBJECTIVES:
- To understand the new paradigm of objects interacting with people, information systems and with other objects
- To introduce various IoT protocols
- To understand the issues in developing specific real time systems on various IoT platforms

COURSE OUTCOMES: After completion of the course, students should be able to
CO-1: Identify and describe different kinds of internet-connected products developed on various IoT platforms
CO-2: Appreciate the challenges involved in establishing user-interaction with connected-objects
CO-3: Develop prototype IoT application using python

UNIT-I:
Introduction to Internet of Things: Definition and Characteristics of IoT, Physical Design of IoT – IoT Architecture, Smart Objects, Bits and Atoms, IoT enabled Technologies – Wireless Sensor Networks, Cloud Computing, Big data analytics, Communication protocols, Embedded Systems.

UNIT-II:
IoT Standards and Protocols: Infrastructure (ex: 6LowPAN, IPv4/IPv6, RPL); Identification (ex: EPC, uCode, IPv6, URIs); Comms / Transport (ex: Wifi, Bluetooth, LoRa); Discovery (ex: Physical Web, mDNS, DNS-SD); Data Protocols (ex: MQTT, CoAP, AMQP, Websocket, Node); Device Management (ex: TR-069, OMA-DM); Semantic (ex: JSON-LD, Web Thing Model); Multi-layer Frameworks (ex: Alljoyn, IoTivity, Weave, Homekit).

UNIT-III:
Introduction to Python: Language features of Python, Data types, data structures, Control of flow, functions, modules, packaging, file handling, data/time operations, classes, Exception handling Python packages - JSON, XML, HTTPLib, URLLib, SMTPLib

UNIT-IV:
IoT Physical Devices and Endpoints: Introduction to Raspberry PI-Interfaces (serial, SPI, I2C) Programming – Python program with Raspberry PI with focus of interfacing external gadgets, controlling output, and reading input from pins.

UNIT-V:
IoT Platforms: Introduction to IoT Platforms (AWS IoT, IBM Watson, ARM Mbed), Cloud Storage models and communication APIs, Python web application framework Designing a RESTful web API.

UNIT-VI:
Iot Applications and Issues: Combination scenarios, Breaking assumptions: - Home, City, Environment, Energy, Retail, Logistics, Agriculture, Industry, health and Lifestyle with Case Studies

TEXT BOOKS:

1. Internet of Things - A Hands-on Approach, Arshdeep Bahga and Vijay Madisetti, Universities Press, 2015, ISBN: 9788173719547
2. Internet of Things: Converging Technologies for Smart Environments and Integrated Ecosystems, Dr. Ovidiu Vermesan, Dr. Peter Friess, River Publishers, 2007
3. Building the Internet of Things. Sara Cordoba, WimerHazenberg, Menno Huisman. BIS Publishers. 2011

REFERENCES:

1. Designing the Internet of Things, Adrian Mcewen, Hakin Cassimally, 2015
2. The Internet of Things: Key Applications and Protocols, Olivier Hersent, David Boswarthick, Omar Elloumi, 2012
3. Getting Started with Raspberry Pi, Matt Richardson & Shawn Wallace, O'Reilly (SPD), 2014, ISBN: 9789350239759
4. Securing the Internet of Things: A Standardization Perspective, Keoh, Sye Loong, Sahoo Subhendu Kumar, and Hannes Tschofenig, Internet of Things Journal, IEEE 1.3 (2014): 265-275

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M.Tech. I Semester (VLSI)	**L**	**T/P**	**C**
	3	**0**	**3**

(A18PE1VS01) FULL CUSTOM IC DESIGN

COURSE PRE-REQUISITES: VLSI Design Concepts, PLDs

COURSE OBJECTIVES:
- To discuss the full custom IC Design flow
- To understand standard cell design techniques
- To understand design methodology

COURSE OUTCOMES: After completion of the course, students should be able to
CO-1: Describe Full Custom CMOS VLSI fabrication Process
CO-2: Design digital system using full custom
CO-3: Develop ASIC Model

UNIT-I:
Types Of Asics – Design flow – Economics of ASICs – ASIC cell libraries – CMOS logic cell data path logic cells – I/O cells – cell compilers.

UNIT-II:
ASIC Library Design: Transistors as resistors – parasitic capacitance – logical effort Programmable ASIC design software: Design system – logic synthesis – half gate ASIC.

UNIT-III:
Low Level Design Entry: Schematic entry – low level design languages – PLA tools – EDIF –An overview of VHDL and Verilog. Logic synthesis in Verilog and & VHDL simulation. CMOS System case studies: Dynamic warp processor: Introduction, the problem, the algorithm, a functional overview, detailed functional specification, structural floor plan, physical design, fabrication, pixels- planes graphic engine: introduction, raster scan graphic fundamental, pixels-planes system overview, chip electrical design, chip organization and layout, clock distribution.

UNIT-IV:
Hierarchical Layout and Design of Single Chip 32 Bit CPU: Introduction, design methodology, technology updatability and layout verification.

UNIT-V:
Floor Planning & Placement: Floor Planning Goals and Objectives, Measurement of Delay in floor planning, Floor planning tools ,I/O and Power planning, Clock planning ,Placement Algorithms.

UNIT-VI:
Routing: Global routing, Detailed routing, special routing.

TEXT BOOKS:
1. Application Specific Integrated Circuits, J. S. Smith, Addison Wesley, 1997
2. Principles of CMOS VLSI Design: A System Perspective, N. Westle & K. Eshraghian, Addison – Wesley Pub.Co.,1985

REFERENCES:
1. Basic VLSI Design: Systems and Circuits, Douglas A. Pucknell & Kamran Eshraghian, Prentice Hall of India Private Ltd., New Delhi, 1989
2. Introduction to VLSI System, C. Mead & L. Canway, Addison Wesley Pub, 1980

3. Introduction to NMOS & VLSI System Design, A. Mukharjee, Prentice Hall, 2015
4. The Design & Analysis of VLSI Circuits, L. A. Glassey& D. W. Dobbepahl, Addison Wesley Pub Co. 1985
5. Digital Integrated Circuits: A Design Perspective, Jan A. Rabey, Prentice Hall of India Pvt Ltd, 2002

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M.Tech. I Semester (VLSI)	**L**	**T/P**	**C**
	3	**0**	**3**

(A18PE1VS02) VLSI PROCESS TECHNOLOGY

COURSE PRE-REQUISITES: Knowledge of MOS Technology and Fabrication Techniques

COURSE OBJECTIVES:
- To provide foundation in MOS and CMOS fabrication process
- To know different lithography methods and etching process
- To study various deposition and diffusion mechanisms
- To understand about packaging of VLSI devices

COURSE OUTCOMES: After completion of the course, students should be able to
CO-1: Appreciate the various techniques involved in the VLSI fabrication process
CO-2: Understand the different lithography methods and etching process
CO-3: Appreciate the deposition and diffusion mechanisms
CO-4: Analyses the fabrication of NMOS, CMOS memory and bipolar devices

UNIT-I:
Electron grade silicon. Crystal growth. Wafer preparation. Vapor phase and molecular beam epitaxy. SOI. Epitaxial evaluation. Oxidation techniques, systems and properties. Oxidation defects.

UNIT-II:
Optical, electron, X-ray and ion lithography methods. Plasma properties, size, control, etch mechanism, etch techniques and equipments.

UNIT-III:
Deposition process and methods. Diffusion in solids. Diffusion equation and diffusion mechanisms.

UNIT-IV:
Ion implantation and metallization. Process simulation of ion implementation, diffusion, oxidation, epitaxy, lithography, etching and deposition. NMOS, CMOS, MOS memory and bipolar IC technologies. IC fabrication.

UNIT-V:
Analytical and assembly techniques. Packaging of VLSI devices.

UNIT-VI:
Plasma and Rapid Thermal Processing: PECVD, Plasma etching and RIE techniques; RTP techniques for annealing, growth and deposition of various films for use in ULSI. Process integration for NMOS, CMOS and Bipolar circuits; Advanced MOS technology

TEXT BOOKS:
1. VLSI Technology, S. M. Sze, 2nd Edition, McGraw Hill, 1988
2. Modern VLSI Design, W. Wolf, 3rd Edition, Pearson, 2002

REFERENCES:
1. VLSI fabrication Principles, S. K. Gandhi, John Wiley Inc., New York, 1983
2. VLSI Fabrication Technology, B. Raj & Singh, Laxmi Publications, 2014
3. VLSI Technology, B. G. Streetman, Prentice Hall, 1990
4. Physics and Technology of Semiconductor Devices, A. S. Grove, John Wiley & Sons, 2008

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M.Tech. I Semester (VLSI)	**L**	**T/P**	**C**
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(A18PE1ES04) PARALLEL PROCESSING

COURSE PRE-REQUISITES: None

COURSE OBJECTIVES:
- To provide an overview of concepts and issues of parallel architectures, models, algorithms and software
- To provide a foundation and context from which current research in Parallel Computation can be understood
- To introduce the principles of developing efficient parallel algorithms

COURSE OUTCOMES: After completion of the course, students should be able to
CO-1: Identify limitations of different architectures of computer
CO-2: Analyze quantitatively the performance parameters for different computer architectures
CO-3: Investigate software issues related to different computer architectures

UNIT-I:
Overview of Parallel Processing and Pipelining, Performance analysis, Scalability.

UNIT-II:
Principles and implementation of Pipelining, Classification of pipelining processors, Advanced pipelining techniques, Software pipelining.

UNIT-III:
Parallel algorithms for multiprocessors- Classification and performance of parallel algorithms, operating systems for multiprocessors systems, Message passing libraries for parallel programming interface, PVM (in distributed memory system), Message Passing Interfaces (MPI).

UNIT-IV:
Multithreaded Architecture, Multithreaded processors, Latency hiding techniques, Principles of multithreading, Issues and solutions.

UNIT-V:
Parallel Programming Techniques: Message passing program development, Synchronous and asynchronous message passing, Shared Memory Programming, Data Parallel Programming, Parallel Software Issues.

UNIT-VI:
Operating systems for multiprocessors systems, customizing applications on parallel processing platforms.

TEXT BOOKS:
1. Computer Architecture and Parallel Processing, Kai Hwang, Faye A. Briggs, MGH International Edition, 2009
2. Advanced Computer Architecture, Kai Hwang, TMH, 2007
3. Computer Organization and Architecture, Designing for Performance, William Stallings, Sixth Edition, Prentice Hall, 2003

REFERENCES:
1. Scalable Parallel Computing, Kai Hwang, Zhiwei Xu
2. High-Performance Computer Architecture, MGH Harold S. Stone, Addison-Wesley, 1993

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M.Tech. I Semester (VLSI)	**L**	**T/P**	**C**
	3	**0**	**3**

(A18PE1VS03) ADVANCED DIGITAL SIGNAL PROCESSING

COURSE PRE-REQUISITES: Knowledge of Digital Filter Design techniques, Digital Signal Processing techniques

COURSE OBJECTIVES:
- To introduce the principles of Multi-rate digital signal processing and its implementation
- To provide ability to compute the power spectrum of the given discrete signal
- To understand various sources of errors affecting the performance of a DSP system
- To understand the necessity of adaptive signal processing

COURSE OUTCOMES: After completion of the course, students should be able to
CO-1: Appreciate the design of multi rate DSP systems
CO-2: Explain the methods of power spectrum estimation of the given signal
CO-3: Comprehend the effect of data word length on the performance of a DSP system
CO-4: Appreciate the applications of adaptive signal processing

UNIT-I:
Review of DFT, FFT, IIR Filters, FIR Filters: Multi-rate Signal Processing: Introduction, Decimation by a factor D, Interpolation by a factor I, Sampling rate conversion by a rational factor I/D, Multistage Implementation of Sampling Rate Conversion, Filter design &Implementation for sampling rate conversion, Applications of Multi-rate Signal Processing.

UNIT-II:
Non-Parametric Methods of Power Spectral Estimation: Estimation of spectra from finite duration observation of signals, Non-parametric Methods: Bartlett, Welch & Blackman & Tukey methods, Comparison of all Non-Parametric methods

UNIT-III:
Linear Prediction and Optimum Linear Filters: Forward and Backward Linear Prediction – Forward Linear Prediction, Backward Linear Prediction, Optimum reflection coefficients for the Lattice Forward and Backward Predictors. Solution of the Normal Equations: Levinson Durbin Algorithm, Schur Algorithm. Properties of Linear Prediction Filters. FIR Wiener Filter, Orthogonality Principle in Linear Mean -Square Estimation.

UNIT-IV:
Parametric Methods of Power Spectrum Estimation: Autocorrelation & Its Properties, Relation between auto correlation & model parameters, AR Models - Yule-Waker & Burg Methods, MA & ARMA models for power spectrum estimation.

UNIT-V:
Finite Word Length Effects: Analysis of finite word length effects in Fixed-point DSP systems – Fixed, Floating Point Arithmetic – ADC quantization noise & signal quality – Finite word length effect in IIR digital Filters – Finite word-length effects

UNIT-VI:
Adaptive Filters: Gradient search Approach, Least Mean Square Algorithm, Recursive Least Squares, Kalman Filters Innovations Process, Estimation of the State Using the Innovations Process, Kalman Filter as the Unifying Basis for RLS Filters, Variations of the Kalman Filter. Applications of Adaptive Filters- System Identification or System Modelling, Adaptive Channel

Equalization, Echo Cancellation in Data Transmission over Telephone Channels, Adaptive Noise Cancelling.

TEXT BOOKS:

1. Digital Signal Processing: Principles, Algorithms & Applications, J. G. Proakis & D. G. Manolokis, 4th Ed., PHI, 2001
2. Adaptive Filter Theory, S. Haykin Pearson, 2003
3. DSP–A Practical Approach, Emmanuel C. I. feacher, Barrie. W. Jervis, 2nd Ed., Pearson Education, 2008

REFERENCES:

1. Modern Spectral Estimation: Theory & Application, S. M. Kay, 1988, PHI
2. Multirate Systems and Filter Banks, P. P. Vaidyanathan, Pearson Education, 1993
3. Digital Signal Processing, S. Salivahanan, A. Vallavaraj, C.Gnanapriya, 2000, TMH

VNR VIGNANA JYOTHI INSTITUTE OF ENGINEERING AND TECHNOLOGY

M.Tech. I Semester (VLSI)	**L**	**T/P**	**C**
	3	**0**	**3**

(A18PE1VS04) SEMICONDUCTOR DEVICE MODELING

COURSE PRE-REQUISITES: Knowledge of Semiconductor Devices

COURSE OBJECTIVES:
- To study the operation of semiconductor devices
- To understand advanced semiconductor devices and technologies
- To learn various models of semiconductor devices
- To understand the BJT, MOSFET and other semiconductor devices from the device modeling perspective

COURSE OUTCOMES: After completion of the course, students should be able to
CO-1: Analyze and describe the characteristics of various diodes
CO-2: Understand the development of complex device models
CO-3: Implement various device models in spice simulation
CO-4: Understand the fabrication techniques involved in VLSI applications

UNIT-I:
Introduction to Semiconductor Physics: Review of Quantum Mechanics, Boltzman transport equation, Continuity equation, Poisson equation.
Integrated Passive Devices: Types and Structures of resistors and capacitors in monolithic technology, Dependence of model parameters on structures

UNIT-II:
Integrated Diodes: Junction and Schottky diodes in monolithic technologies – Static and Dynamic behavior – Small and large signal models – SPICE models
Integrated Bipolar Transistor: Types and structures in monolithic technologies – Basic model (Eber-Moll) – Gunmel- Poon model dynamic model, Parasitic effects – SPICE model– Parameter extraction

UNIT-III:
Bipolar Junction Transistors: Structure of a BJT, carrier statistics in base, emitter, collector, figures of merit, basic principle of operation, long base transistor, short base transistor, analysis of ideal diffusion transistor, Ebers-Moll model
Bipolar Device Design: Design of the emitter design, Design of the base region, Design of the collector design, Modern bipolar transistor structures.

UNIT-IV:
Integrated MOS Transistor: NMOS and PMOS transistor, Threshold voltage, Threshold voltage equations, MOS device equations, Basic DC equations second order effects, MOS models, small signal AC characteristics, MOSFET SPICE model level 1, 2, 3 and 4.

UNIT-V:
VLSI Fabrication Techniques: An overview of wafer fabrication, Wafer Processing, Oxidation, Patterning, Diffusion, Ion Implantation, Deposition, Silicon gate NMOS process, CMOS processes, n-well- p-well- twin tub- Silicon on insulator, CMOS process enhancements, Interconnects circuit elements.

UNIT-VI:
Modeling of Hetero Junction Device: Band gap Engineering, Band gap Offset at abrupt Hetero Junction, Modified current continuity equations, Hetero Junction bipolar transistors (HBTs), SiGe

TEXT BOOKS:

1. Introduction to Semiconductor Materials and Devices, Tyagi M. S., John Wiley Student Edition, 2008
2. Solid State Circuits, Ben G. Streetman, Prentice Hall, 1997

REFERENCES:

1. Physics of Semiconductor Devices, Sze S. M., 2nd Edition, McGraw Hill, New York, 1981
2. Introduction to Device Modeling and Circuit Simulation, Tor A. Fijedly, Wiley-Inderscience, 1997
3. Introduction to VLSI Systems: A Logic, Circuit and System Perspective, Ming-BO Lin, CRC Press, 2011

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M.Tech. I Semester (VLSI)	**L**	**T/P**	**C**
	0	**3**	**1.5**

(A18PC2VS01) SIMULATION AND SYNTHESIS WITH PLDs LABORATORY

COURSE PRE-REQUISITES: Digital Concepts, Programming Knowledge

COURSE OBJECTIVES:
- To provide familiarity with hardware description language Verilog HDL for modelling of combinational and sequential circuits
- To understand the role of functional simulator in the validating the functionality of designed circuits
- To understand the Synthesis of a designed digital circuits
- To introduce the process of implementation of digital circuits on FPGA kits

COURSE OUTCOMES: After completion of the course, students should be able to
CO-1: Apply CAD tools for the design of digital circuits
CO-2: Appreciate the process of synthesizing a given digital circuits
CO-3: Implement the specified digital circuits using FPGA

LIST OF EXPERIMENTS:

Implementation of the following designs on FPGA using Verilog HDL:

1. 8:1 Mux/Demux, Full Adder, 8-bit Magnitude comparator, Encoder/decoder, Priority encoder, Parity generator
2. Code converters
3. D-FF, 4-bit Shift registers (SISO, SIPO, PISO, bidirectional), 3-bit Synchronous Counters.
4. Sequence generator/detectors, Synchronous FSM – Mealy and Moore machines.
5. Vending machines - Traffic Light controller, ATM, elevator control.
6. PCI Bus &Arbiter.
7. Single and Dual port SRAM
8. Arithmetic circuits like serial adder/ subtractor, parallel adder/subtractor, serial/parallel multiplier.

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M.Tech. I Semester (VLSI)	**L**	**T/P**	**C**
	0	**3**	**1.5**

(A18PC2VS02) IC DESIGN LABORATORY

COURSE PRE-REQUISITES: Concepts of Digital and Analog Circuits

COURSE OBJECTIVES:
- To learn the design procedure of digital and analog circuits using EDA tools
- To understand the design of analog circuit using EDA tools
- To understand how to calculate width of transistors for accurate designs

COURSE OUTCOMES: After completion of the course, students should be able to
CO-1: Design digital circuit using CMOS and other logic styles
CO-2: Compare various designs with respect to performance metrics
CO-3: Design Analog Circuit using CMOS
CO-4: Use EDA tools like Synopsys, Mentor Graphics and other open-source software tools like Hspice

LIST OF EXPERIMENTS:

Implementation of the following designs using CAD Tools:

1. Obtain DC and transient characteristics of CMOS logic gates and draw the equivalent layouts for each gate and perform DRC, LVS and parasitic extraction using CAD tools
2. Design and verify the functionality of 1-bit full adder using PTL and transmission gate logics and compare the performance parameters like power dissipation and speed among various optimized full adder cells
3. Verify the dynamic, domino C2MOS and NPCMOS logic with suitable examples
4. Design and verify the functionalities of clocked latches and flip flop circuits
5. Design the circuits of SRAM, DRAM memory cells and verify its functionality
6. Design of Common source amplifier
7. Design of Wilson current mirror
8. Design of Single stage differential amplifier
9. Design of Operational amplifier

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M.Tech. I Semester (VLSI)	**L**	**T/P**	**C**
	0	**4**	**2**

(A18PW4VS01) TECHNICAL SEMINAR

COURSE OUTCOMES: After completion of the course, students should be able to
CO-1: Identify a research topic related to advanced/state-of-the-art technologies
CO-2: Collect the literature and comprehend/analyze critically the technological advancements
CO-3: Engage in effective oral communication through presentation of seminar
CO-4: Engage in effective written communication through report

COURSE OUTLINE:

- A student shall present a seminar on a technical topic during I semester of the M.Tech. programme.
- A student, under the supervision of a faculty member, shall collect literature on a technical topic of his / her choice, critically review the literature and submit it to the Seminar Review Committee (SRC) in a prescribed report form.
- The SRC shall consist of Head of the Department, faculty supervisor and a senior faculty member of the specialization / department.
- Student shall make an oral presentation before the SRC after clearing the plagiarism check.
- Prior to the submission of seminar report to the SRC, its soft copy shall be submitted to the PG Coordinator for PLAGIARISM check.
- The report shall be accepted for submission to the SRC only upon meeting the prescribed similarity index.

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M.Tech. I Semester (VLSI)	**L**	**T/P**	**C**
	2	**0**	**0**

(A18AU5CS01) RESEARCH METHODOLOGY AND IPR

COURSE PRE-REQUISITES: None

COURSE OBJECTIVES:
- To introduce the characteristics of a good research problem
- To choose appropriate approaches of investigation of solutions for research problem
- To familiarize with basic Intellectual Property Rights
- To understand different Patent Rights

COURSE OUTCOMES: After completion of the course, students should be able to
CO-1: Understand research problem formulation, analyze research related information and follow research ethics
CO-2: Realize the importance of ideas, concept, and creativity in the present-day context
CO-3: Recognize that when IPR would take such important place in growth of individuals and nation, it is needless to emphasize the need of information about IPR to be promoted among students in general and engineering in particular
CO-4: Appreciate IPR protection which leads to creation of new and better products, and in turn brings about, economic growth and social benefits

UNIT-I:
Introduction: Meaning of research problem, Sources of research problem, Criteria Characteristics of a good research problem, Errors in selecting a research problem, Scope and objectives of research problem.
Approaches of investigation of solutions for research problem, data collection, analysis, interpretation, necessary instrumentations.

UNIT-II:
Literature Survey: Effective literature studies approaches, analysis. Plagiarism, Research ethics.

UNIT-III:
Effective Technical Writing: How to write report, Paper. Developing a Research Proposal, Format of research proposal, a presentation and assessment by a review committee

UNIT-IV:
Nature of Intellectual Property: Patents, Designs, Trade and Copyright. Process of
Patenting and Development: technological research, innovation, patenting, development.
International Scenario: International cooperation on Intellectual Property. Procedure for grants of patents, Patenting under PCT.

UNIT-V:
Patent Rights: Scope of Patent Rights. Licensing and transfer of technology. Patent information and databases. Geographical Indications.

UNIT-VI:
New Developments in IPR: Administration of Patent System. New developments in IPR; IPR of Biological Systems, Computer Software etc. Traditional knowledge Case Studies, IPR.

TEXT BOOKS:
1. Research Methodology: An Introduction for Science & Engineering Students, Stuart Melville and Wayne Goddard

2. Research Methodology: An Introduction, Wayne Goddard and Stuart Melville
3. Resisting Intellectual Property, Halbert, Taylor & Francis Ltd ,2007

REFERENCES:

1. Research Methodology: A Step-by-Step Guide for Beginners, Ranjit Kumar, 2nd Edition
2. Research Methodology: Methods and Techniques, C. R. Kothari and Gaurav Garg, New Age International Publishers
3. Intellectual Property in New Technological Age, Robert P. Merges, Peter S. Menell, Mark A. Lemley, 2016
4. Intellectual Property Rights Under WTO, T. Ramappa, S. Chand, 2008

VNR VIGNANA JYOTHI INSTITUTE OF ENGINEERING AND TECHNOLOGY

M.Tech. II Semester (VLSI)	**L**	**T/P**	**C**
	3	**0**	**3**

(A18PC1VS04) MIXED SIGNAL AND RF IC DESIGN

COURSE PRE-REQUISITES: Knowledge on Design of various Analog Circuits

COURSE OBJECTIVES:
- To learn the design of CMOS comparators
- To understand the design and architectures of data converters
- To study the various impedance matching techniques in RF circuit design
- To know the fundamentals and issues in the design of Phase Locked Loop

COURSE OUTCOMES: After completion of the course, students should be able to
CO-1: Learn and compare different types of data converter architectures
CO-2: Design of Nyquist Rate A/D Converters and Oversampling Converters
CO-3: Understand the design issues and challenges involved in PLL and comparator
CO-4: To study the various impedance matching techniques in RF circuit design and frequency synthesis

UNIT-I:
Comparators: Basic CMOS comparator design, Characterization of Comparator, Latched comparators, Clocked Comparator, Two-Stage, Open-Loop Comparators, Analog multipliers.
Data Converter Fundamentals: DC and dynamic specifications, Quantization noise, Nyquist rate D/A converters- Decoder based converters, Binary-Scaled converters, Thermometer-code converters, Hybrid converters

UNIT-II:
Nyquist Rate A/D Converters: Successive approximation converters, Flash converter, Two-step A/D converters, Interpolating A/D converters, Folding A/D converters, Pipelined A/D converters, Time-interleaved converters.

UNIT-III:
Oversampling Converters: Noise shaping modulators, Decimating filters and interpolating filters, Higher order modulators, Delta sigma D/A.

UNIT-IV:
Impedance Matching in Amplifiers: Definition of Q, series parallel transformations of lossy circuits, impedance matching using L, PI and T networks, Integrated inductors, resistors, Capacitors, tunable inductors, transformers.
Amplifier Design: Noise characteristics of MOS devices, Design of CG LNA and inductor degenerated LNAs. Principles of RF Power Amplifiers design.

UNIT-V:
Oscillators: LC Oscillators, Voltage Controlled Oscillators, Ring oscillators, Delay Cells, tuning range in ring oscillators, Tuning in LC oscillators, Tuning sensitivity, Phase Noise in oscillators, sources of phase noise.

UNIT-VI:
PLL and Frequency Synthesizers: Phase Detector/Charge Pump, Analog Phase Detectors, Digital Phase Detectors, Frequency Dividers, Loop Filter Design, Phase Locked Loops, Phase noise in PLL, Loop Bandwidth, Basic Integer-N frequency synthesizer.

TEXT BOOKS:

1. Design of Analog CMOS Integrated Circuits, Behzad Razavi, TMH Edition, 2002
2. CMOS Analog Circuit Design, Philip E. Allen and Douglas R. Holberg, Oxford University Press, International Second Edition / Indian Edition, 2010
3. RF Microelectronics, B. Razavi, Prentice-Hall, 1998

REFERENCES:

1. CMOS Integrated Analog-to-Digital and Digital-to-Analog Converters, Rudy Van De Plassche, Kluwer Academic Publishers, 2003
2. Understanding Delta-Sigma Data Converters, Richard Schreier, Wiley Interscience, 2005
3. CMOS Mixed-Signal Circuit Design, R. Jacob Baker, Wiley Interscience, 2009
4. Microstrip Filters for RF/Microwave Applications, Jia-sheng Hong, Wiley, 2001

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M.Tech. II Semester (VLSI)	**L**	**T/P**	**C**
	3	**0**	**3**

(A18PC1VS05) VLSI DESIGN FOR VERIFICATION AND TESTING

COURSE PRE-REQUISITES: Concepts of VLSI and Digital Design

COURSE OBJECTIVES:
- To verify VLSI designs using System Verilog language concepts
- To understand various testing techniques
- To learn Fault Modeling, fault simulation algorithms and testability measures for VLSI circuits
- To study various scan design techniques for digital systems

COURSE OUTCOMES: After completion of the course, students should be able to
CO-1: Develop verification methods using System Verilog concepts
CO-2: Apply the testing concepts to achieve better yield in IC design
CO-3: Analyze different fault models, simulation algorithms and testable measures
CO-4: Identify scan designs, BIST architectures and boundary scan standards

UNIT-I:
Introduction to Verification using System Verilog: System Verilog Literal Values and Built-in Data Types, User-Defined and Enumerated Types, System Verilog Arrays, Structures and Unions, Operators in System Verilog, Procedural Blocks, Loops.

UNIT-II:
Arrays: Packed and Unpacked Arrays, Dynamic Arrays, Associative Arrays, Queues, examples, Test bench and Design, System Verilog Assertions, BASIC OOPs, classes, class object and handles, examples, Randomization, examples.

UNIT-III:
Introduction to Testing: Role of Testing, VLSI Technology Trends affecting Testing, Types of Testing, Fault Modeling: Defects, Errors and Faults, Functional Versus Structural Testing, Levels of Fault Models, Single Stuck-at Fault, Test generation – Random test generation, Path sensitization techniques, Boolean Difference method.

UNIT-IV:
Logic and Fault Simulation: Simulation for Design Verification, Fault simulation for test and diagnosis, Simulation models-Gate level network, Logic symbols, Logic element evaluation, Timing models, Logic simulation, Hazards, Fault simulation-serial, parallel, deductive, concurrent and differential fault simulation.

UNIT-V:
DFT: SCOAP Controllability and Observability, Combinational SCOAP Measures Combinational Circuit Example, Sequential SCOAP Measures, Sequential Circuit Example.
Scan Designs: Ad-Hoc approach, structured approach, Scan cell Designs- Mux-D Scan Cell, Clocked-Scan Cell, LSSD Scan Cell, Scan Architectures-Full-Scan Design, Partial Scan Design, Random Access Scan Design, Scan design rules, Scan design flow.

UNIT-VI:
Logic Built-in Self –Test: Introduction, BIST Design Rules, Test pattern generation-Exhaustive testing, Pseudo-Random Testing, Pseudo-Exhaustive Testing, Delay fault testing, Output response Analysis-ones count testing, transition count testing, Signature Analysis, logic BIST Architectures-BIST Architectures for circuits without scan chains, BIST Architectures for circuits with scan chains.

TEXT BOOKS:

1. System Verilog for Design, Stuart Sutherland, Simon Davidmann, Peter Flake, 2nd Edition, Springer, 2006
2. VLSI Test Principles and Architectures: Design for Testability, Laung-Terng, Cheng-Wen Wu, Xiaoqing Wen, I Edition, Morgan Kaufmann, 2006
3. Essentials of Electronic Testing for Digital, Memory and Mixed Signal VLSI Circuits, M. L. Bushnell, V. D. Agrawal, Kluwer Academic Publishers, 2000

REFERENCES:

1. System Verilog for Verification, Chris Spears, 2nd Edition, Springer, 2009
2. Digital System Design using Programmable Logic Devices, Parag K. Lala, Prentice Hall, NJ, 1994
3. Digital Circuits Testing and Testability, P. K. Lala, Academic Press, 2009

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M.Tech. II Semester (VLSI)	**L**	**T/P**	**C**
	3	**0**	**3**

(A18PC1VS06) LOW POWER VLSI DESIGN

COURSE PRE-REQUISITES: Basic concepts of Digital Systems

COURSE OBJECTIVES:
- To understand the low power issues in VLSI circuits
- To design various circuits for optimize power
- To understand case study of low power design

COURSE OUTCOMES: After completion of the course, students should be able to
CO-1: Identify the sources of power dissipation in digital IC systems
CO-2: Understand the impact of power on system performance and reliability
CO-3: Characterize and model power consumption & understand the basic analysis methods
CO-4: Understand leakage sources and reduction techniques

UNIT-I:
Technology & Circuit Design Levels: Sources of power dissipation in digital ICs, degree of freedom, recurring themes in low-power, emerging low power approaches, dynamic dissipation in CMOS, effects of VDD & VT on speed, constraints on VT reduction, transistor sizing & optimal gate oxide thickness, impact of technology scaling, technology innovations.

UNIT-II:
Low Power Circuit Techniques: Power consumption in circuits, flip-flops & latches, high capacitance nodes, energy recovery, reversible pipelines, high performance approaches.

UNIT-III:
Low Power Clock Distribution: Power dissipation in clock distribution, single driver Versus distributed buffers, buffers & device sizing under process variations, zero skew Vs. tolerable skew, chip & package co-design of clock network.

UNIT-IV:
Logic Synthesis for Low Power Estimation Techniques: Power minimization techniques, low power arithmetic components- circuit design styles, adders- Ripple Carry Adders, Carry Look-Ahead Adders, Carry Select Adders, Carry Save Adders, multipliers- Braun Multiplier, Baugh-Wooley Multiplier, Booth Multiplier.

UNIT-V:
Low Power Memory Design: Sources & reduction of power dissipation in memory subsystem, sources of power dissipation in DRAM & SRAM, low power DRAM circuits, low power SRAM circuits.

UNIT-VI:
Low Power Microprocessor Design System: Power management support, architectural tradeoffs for power, choosing the supply voltage, low- power clocking, implementation problem for low power, comparison of microprocessors for power & performance.

TEXTBOOKS
1. Low Power Design Methodologies, Jan M. Rabaey, 1st Edition, Springer, 2010
2. Low Power CMOS VLSI Circuit Design, Kaushik Roy, Sharat Prasad, John Wiley Sons Inc., 2000

REFERENCES:

1. Low Power VLSI Circuits and Systems, Pal Ajit, Springer, 2015
2. Low Voltage CMOS VLSI Circuits, J. B. Kulo and J. H. Lou, Wiley, 1999
3. Low Power Digital CMOS Design, A. P. Chandrasekaran and R. W. Broadersen, Kluwer,1995
4. Practical Low Power Digital VLSI Design, Gary Yeap, Kluwer, 1998

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M.Tech. II Semester (VLSI)	**L**	**T/P**	**C**
	3	**0**	**3**

(A18PE1ES06) SOC AND NOC ARCHITECTURES

COURSE PRE-REQUISITES: None

COURSE OBJECTIVES:
- To understand the principles of system on chip design and its applications
- To introduce the design principles of NOC
- To understand the various computation models of SOC and NOC design

COURSE OUTCOMES: After completion of the course, students should be able to
CO-1: Appreciate the design of a system architecture for the given performance indicators such as Power, Performance, Area
CO-2: Differentiate and explain the principles of SOC and NOC design
CO-3: Explain the role of system-level design and performance metrics in choosing a SOC/NOC design

UNIT-I:
Introduction to SoC Design. Multiprocessor SOC and Network on Chip. Low-Power SoC Design.

UNIT-II:
System Design: Co-Design using System Models Validation and Verification, Hardware/Software Co-Design Application Analysis, Synthesis.

UNIT-III:
Communication System: Separation of Computation and Communication. Communication-Centric SOC Design, Communication Synthesis. Network-Based Design, Network on Chip, Architecture of NOC.

UNIT-IV:
NOC Topology & Protocol Design: Analysis Methodology, NoC Topology, Energy Exploration, NOC Protocol Design.

UNIT-V:
Low-Power Design for NOC: Low-Power Signalling, On-Chip Serialization, Low-Power Clocking, Low-Power Channel Coding, Low-Power Switch, Low-Power Network on Chip Protocol.

UNIT-VI:
Example SOC/NOC Designs: Real Chip Implementation, Industrial Implementations, Intel's Tera-FLOP 80-Core NOC, Intel's Scalable Communication Architecture, Design case studies.

TEXT BOOKS:
1. Low Power NoC for High Performance SoC Design, Hoi-Junyoo, Kangmin Lee, Jun Kyoungkim, CRC Press, 2008
2. A Platform-Centric Approach to System-on-Chip (SOC) Design, Vijay K. Madisetti, Chonlameth Arpikanondt, Springer, 2005

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M.Tech. II Semester (VLSI)	**L**	**T/P**	**C**
	3	**0**	**3**

(A18PE1VS05) OPTIMIZATION TECHNIQUES IN VLSI DESIGN

COURSE PRE-REQUISITES: Low Power VLSI Design, Device Modeling and CAD for VLSI

COURSE OBJECTIVES:
- To understand various statistical Modeling methodologies
- To analyze different estimation techniques
- To learn concepts of optimization algorithms
- To compare performance of systems in terms of power

COURSE OUTCOMES: After completion of the course, students should be able to
CO-1: Apply the appropriate design modeling practices for emerging IC technologies
CO-2: Design the systems by using statistical analysis methods
CO-3: Design the low power digital systems by applying appropriate partitioning and Floor planning algorithms
CO-4: Design the real time applications using optimization techniques like Genetic Algorithms

UNIT-I:
Statistical Modeling: Modeling sources of variations, Monte Carlo techniques, Process variation Modeling- Pelgrom's model, Principle component-based modeling, Quad tree based modeling, Performance modeling-Response surface methodology, delay modeling, interconnect delay models.

UNIT-II:
Statistical Performance, Power and Yield Analysis: Statistical timing analysis, parameter space techniques, Bayesian networks Leakage models, High level statistical analysis, Gate level statistical analysis, dynamic power, leakage power, temperature and power supply variations, High level yield estimation and gate level yield estimation.

UNIT-III:
Convex Optimization: Convex sets, convex functions, geometric programming, trade-off and sensitivity analysis, Generalized geometric programming, geometric programming applied to digital circuit gate sizing, Floor planning, wire sizing, Approximation and fitting- Monomial fitting, Maxmonomial fitting, Posynomial fitting.

UNIT-IV:
Genetic Algorithm: Introduction, GA Technology-Steady State Algorithm-Fitness Scaling-Inversion GA for VLSI Design, Layout and Test automation- partitioning-automatic placement, routing technology, Mapping for FPGA- Automatic test generation- Partitioning algorithm Taxonomy-Multi-way Partitioning Hybrid genetic- encoding-local improvement-WDFR Comparison of CAS-Standard cell placement-GASP algorithm- unified algorithm.

UNIT-V:
GA Routing Procedures: Global routing-FPGA technology mapping-circuit generation-test generation in a GA frame work-test generation procedure.

UNIT-VI:
Power Estimation: Power estimation-application of GA-Standard cell placement-GA for ATG-problem encoding- fitness function-GA vs. Conventional algorithm.

TEXT BOOKS:

1. Statistical Analysis and Optimization for VLSI: Timing and Power, Ashish Srivastava, Dennis Sylvester, David Blaauw, Springer, 2005
2. Genetic Algorithm for VLSI Design, Layout and Test Automation, Pinaki Mazumder, E. Mrudnick, Prentice Hall, 1998
3. Convex Optimization, Stephen Boyd, Lieven Vandenberghe, Cambridge University Press, 2004

REFERENCES:

1. VLSI Digital Signal Processing Systems, Keshab K. Parhi, Wiley, 2015
2. Logic in Computer Science Modeling and Reasoning about Systems, M. Huth and M. Ryan, Cambridge University Press, 2004
3. Essentials of Electronic Testing for Digital, Memory & Mixed, Signal Circuits, Bushnell and Agrawal, Kluwer Academic Publishers, 2000

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M.Tech. II Semester (VLSI)	**L**	**T/P**	**C**
	3	**0**	**3**

(A18PE1VS06) SCRIPTING LANGUAGES FOR VLSI

COURSE PRE-REQUISITES: Linux Basics, Basics of C

COURSE OBJECTIVES:
- To understand the importance of scripting languages in VLSI Design
- To describe the various PERL concepts used in VLSI design for large data handling
- To understand utilization of TCL in CAD Tools Interfacing
- To interpret PYTHON language

COURSE OUTCOMES: After completion of the course, students should be able to
CO-1: Gain fluency in programming with scripting languages
CO-2: Create and run scripts using PERL/TCL/PYTHON in CAD Tools
CO-3: Demonstrate the use of PERL/PYTHON/ TCL in developing system and web applications

UNIT-I:
Introduction to Scripts and Scripting: Basics of Linux, Origin of Scripting languages, scripting today, Characteristics and uses of scripting languages.

UNIT-II:
PERL: Introduction to PERL, Names and values, Variables and assignment, Scalar expressions, Control structures, Built-in functions, Collections of Data, Working with arrays, Lists and hashes, Simple input and output, Strings, Patterns and regular expressions, Subroutines, Scripts with arguments.

UNIT-III:
Advanced PERL: Finer points of Looping, Subroutines, Using Pack and Unpack, Working with files, Type globs, Eval, References, Data structures, Packages, Libraries and modules, Objects, Objects and modules in action, Tied variables, interfacing to the operating systems, Security issues.

UNIT-IV:
TCL: The TCL phenomena, Philosophy, Structure, Syntax, Parser, Variables and data in TCL, Control flow, Data structures, Simple input/output, Procedures, Working with Strings, Patterns, Files and Pipes, Example code.

UNIT-V:
Advanced TCL: The eval, source, exec and up-level commands, Libraries and packages, Namespaces, Trapping errors, Event-driven programs, Making applications 'Internet-aware', 'Nuts-and-bolts' internet programming, Security issues, TCL and TK integration.

UNIT-VI:
PYTHON: Introduction to PYTHON language, PYTHON-syntax, statements, functions, Built-in-functions and Methods, Modules in PYTHON, Exception Handling.

TEXT BOOKS:
1. The World of Scripting Languages, David Barron, Wiley Student Edition, 2010
2. PYTHON Web Programming, Steve Holden and David Beazley, New Riders Publications

REFERENCES:

1. TCL/TK: A Developer's Guide, Clif Flynt, Morgan Kaufmann Series, 2003
2. Core PYTHON Programming, Chun, Pearson Education, 2006
3. Learning Perl, Randal L. Schwartz, 6th Edition, O' Reilly Publications, 2011
4. Linux: The Complete Reference, Richard Peterson, 6th Edition, McGraw Hill, 2008

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M.Tech. II Semester (VLSI)	**L**	**T/P**	**C**
	3	**0**	**3**

(A18PE1VS07) PHYSICAL DESIGN AUTOMATION

COURSE PRE-REQUISITES: Basic concepts of Digital Systems

COURSE OBJECTIVES:
- To know VLSI Physical Design Automation
- To learn concepts related to physical design like floor planning, partitioning and placement
- To learn concepts related to physical design like routing and different routing techniques and compaction algorithms

COURSE OUTCOMES: After completion of the course, students should be able to
CO-1: Study automation process for VLSI System design
CO-2: Understanding of fundamentals for various physical design CAD tools
CO-3: Develop and enhance the existing algorithms and computational techniques for physical design process of VLSI systems

UNIT-I:
Introduction to VLSI Physical Design Automation: Design Representation, VLSI Design Styles, and VLSI Physical Design automation.

UNIT-II:
Partitioning, Floor planning, Pin Assignment, Standard cell, Performance issues in circuit layout, delay models, Layout styles.

UNIT-III:
Placement: Problem formulation, classification, Simulation based placement algorithms, Partitioning based placement algorithms, Time driven and performance driven placement.

UNIT-IV:
Global Routing: Problem formulation, classification of global routing, Maze routing algorithms, Line- Probe algorithms, and shortest path-based algorithms, Steiner Tree based algorithms, Integer programming-based approach, Performance driven routing.
Detailed Routing: Problem formulation, classification, Single layer, two-layer, three layer and Multi-Layer channel routing, Algorithms, Switch box routing.

UNIT-V:
Over the Cell Routing - Single Layer and Two-Layer Routing: Over the cell routing, Two Layer, Three Layer and Multi-Layer OTC Routing.
Via Minimization: Constraint and Unconstrained via minimization.
Clock and Power Routing: Clocking schemes, design considerations for the clock, Problem formulation, Clock routing algorithms, Skew and Delay reduction by Pin Assignment, Multiple clock routing, Power and Ground Routing

UNIT-VI:
Compaction Algorithms: Problem formation, Classification of compaction algorithms, One dimensional compaction, two-dimensional compaction, 1-1/2 dimensional compaction, Hierarchical compaction, recent trends in compaction.
Physical Design Automation of FPGAs and MCM's: Technologies, physical design cycle, partitioning, placement, routing.

TEXT BOOKS:

1. Algorithms for VLSI Physical Design Automation, Naveed Sherwani, 3rd Ed., 2005
2. Algorithms for VLSI Design Automation, S. H. Gerez, 1999, Wiley Student Edition, John Wiley & Sons (Asia) Pvt. Ltd.

REFERENCES:

1. Computer Aided Logical Design with Emphasis on VLSI, Hill & Peterson, 1993, Wiley
2. Modern VLSI Design: Systems on Silicon, Wayne Wolf, 2nd ed., 1998, Pearson Education Asia

VNR VIGNANA JYOTHI INSTITUTE OF ENGINEERING AND TECHNOLOGY

M.Tech. II Semester (VLSI)	**L**	**T/P**	**C**
	3	**0**	**3**

(A18PE1VS08) IMAGE AND VIDEO PROCESSING

COURSE PRE-REQUISITES: None

COURSE OBJECTIVES:
- To introduce the fundamental differences between image and video processing
- To understand various filtering operations essential for image/video processing
- To introduce the concept of compression with reference to image and video
- To introduce the principles of multi-dimensional estimation with reference to a video signal

COURSE OUTCOMES: After completion of the course, students should be able to
CO-1: Understand the fundamentals of digital image processing
CO-2: Appreciate the advantages of compression in image /video processing
CO-3: Understand the concepts of video formation, sampling and representation
CO-4: Understand the principles of motion estimation in a video

UNIT-I:
Fundamentals of Image Processing: Basic steps of Image processing system sampling and quantization of an Image – Basic relationship between pixels
Image Transforms: 2 – D Discrete Fourier Transform, Discrete Cosine Transform (DCT), Introduction to wavelet Transform, Continuous wavelet Transform, Discrete wavelet Transform, Filter banks

UNIT-II:
Image Enhancement:
Spatial Domain Methods: Histogram Processing, Fundamentals of Spatial Filtering, Smoothing Spatial filters, Sharpening Spatial filters
Frequency Domain Methods: Basics of filtering in frequency domain, image smoothing, image sharpening, selective filtering

UNIT-III:
Segmentation: Segmentation concepts, Point, Line and Edge Detection, Edge Linking using Hough Transform, Thresholding, Region Based segmentation.
Morphological Image Processing
Dilation and Erosion, Opening and closing, the hit or miss Transformation, Overview of Digital Image Watermarking Methods

UNIT-IV:
Image Compression: Image compression fundamentals – Coding Redundancy, Spatial and Temporal Redundancy. Compression Models: Lossy and Lossless, Huffmann Coding, Arithmetic Coding, LZW Coding, Run Length Coding, Bit Plane Coding, Transform Coding, Predictive Coding, Wavelet Coding, Wavelet Based Image Compression, JPEG standards.
Image Restoration: Degradation Models, PSF, Circulant And Block - Circulant Matrices, Deconvolution, Restoration Using Inverse Filtering, Wiener Filtering.

UNIT-V:
Basic Steps of Video Processing: Analog video, Digital Video, Time varying Image Formation Models: 3D Motion Models, Geometric Image Formation, Photometric Image Formation, Sampling of Video Signals, Filtering Operations

UNIT-VI:

2-D Motion Estimation: Optical Flow, General Methodologies, Pixel Based Motion Estimation, Block Matching Algorithm, Mesh based Motion Estimation, Global Motion Estimation, Region based Motion Estimation, Multi Resolution Motion Estimation. Waveform based Coding, Block based Transform Coding, Predictive Coding, Application of Motion Estimation in video Coding.

TEXT BOOKS:

1. Digital Image Processing, Gonzaleze and Woods, 3rd Ed., Pearson
2. Video Processing and Communication, Yao Wang, Joern Ostermann and Ya-Qin Zhang, I Ed Prentice Hall

REFERENCES:

1. Digital Video Processing, M. Tekalp, Prentice Hall International

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M.Tech. II Semester (VLSI)	**L**	**T/P**	**C**
	3	**0**	**3**

(A18PE1VS09) MEMORY TECHNOLOGIES

COURSE PRE-REQUISITES: Concepts of Digital Electronics, Memory Organization and Design for Testability

COURSE OBJECTIVES:
- To introduce the concepts of memory and its classification
- To understand the issues associated with the selection of application specific memory unit
- To introduce the recent advancements in the design of semiconductor memories

COURSE OUTCOMES: After completion of the course, students should be able to
CO-1: Select architecture and design semiconductor memory circuits and subsystems
CO-2: Identify various fault models, modes and mechanisms in semiconductor memories and their testing procedures
CO-3: Knowhow of the state-of-the-art memory chip design

UNIT-I:
Random Access Memory Technologies: Static Random-Access Memories (SRAMs), SRAM Cell Structures, MOS SRAM Architecture, MOS SRAM Cell and Peripheral Circuit operation, Bipolar SRAM technologies, Advanced SRAM Architectures and technologies, Application Specific SRAMs.

UNIT-II:
Dynamic Random-Access Memory: DRAM technology Development, MOS DRAM Cell theory and advanced cell structures, Bi-CMOS DRAM, Error Failures in DRAM, Advanced DRAM Design and Architecture, Application Specific DRAMs. SRAM and DRAM Memory controllers.

UNIT-III:
Non-Volatile Memories: Masked ROMs, High Density ROM, PROMs, Bipolar ROM, CMOS PROM, EEPROMs, Floating Gate EPROM Cell, One-time programmable EPROM, EEPROM technology and architecture, Non-volatile SRAM, Flash Memories.

UNIT-IV:
Semiconductor Memory Reliability and Radiation Effects: General Reliability Issues, RAM Failure modes and mechanism, Non-volatile Memory reliability, reliability modeling and failure rate prediction. Design for reliability, Reliability Test structures, screening and qualification, Radiation Effects, Single Event Phenomenon (SEP), Radiation Hardening Techniques, process and design issues. Radiation Hardened Memory Characteristics, Radiation Hardness Assurance and Testing.

UNIT-V:
Advanced Memory Technologies and High-density Memory Packing Technologies Ferroelectric Random Access Memories
(FRAMs), Gallium Arsenide (GaAs) FRAMs, Analog Memories, Magneto Resistive Random-Access Memories (MRAMs), Experimental Memory Devices.

UNIT-VI:
Memory Hybrids (2D & 3D), Memory Stacks, Memory MCM Testing and Reliability Issues, Memory Cards, High Density Memory Packaging.

TEXT BOOKS:

1. Advanced Semiconductor Memories: Architectures, Designs, and Applications, Ashok K. Sharma, Wiley-IEEE Press, 2002, ISBN: 978-0-471-20813-6
2. VLSI Memory Chip Design, Kiyooltoh, Springer Series, 2001, ISBN 978-3-662-04478-0

REFERENCES:

1. Semiconductor Memories: Technology, Testing and Reliability, Ashok K Sharma, Wiley-Blackwell, 2002
2. Modern Semiconductor Devices for Integrated Circuits, Chenming C. Hu, 1st Edition, 2009

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M.Tech. II Semester (VLSI)	**L**	**T/P**	**C**
	0	**3**	**1.5**

(A18PC2VS03) MIXED SIGNAL AND RF IC DESIGN LABORATORY

COURSE PRE-REQUISITES: Analog and Digital IC Design

COURSE OBJECTIVES:
- To understand the design of mixed circuit using EDA tools
- To understand the accurate design of transistor circuits

COURSE OUTCOMES: After completion of the course, students should be able to
CO-1: Understand the necessity of mixed signal systems
CO-2: Design comparators that can meet the high-speed requirements of digital circuitry
CO-3: Design Mixed Circuit
CO-4: Use EDA tools like Synopsys, Mentor Graphics and other open-source software tools like HSpice

LIST OF EXPERIMENTS:

Implementation of the following designs using CAD Tools:

1. High speed comparator design-Two stage cross coupled clamped comparator
2. Design of High Speed Dynamic Latch Comparator
3. Design of Flash ADC
4. Design of LNA
5. Implementation of VCO
6. Implementation of PFD

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M.Tech. II Semester (VLSI)	**L**	**T/P**	**C**
	0	**3**	**1.5**

(A18PC2VS04) VLSI DESIGN VERIFICATION AND TESTING LABORATORY

COURSE PRE-REQUISITES: Verilog HDL, Digital Design Course

COURSE OBJECTIVES:
- To know digital building blocks, test benches and verify the functionality using HDL
- To Study the Verification concepts using System Verilog
- To learn principles of verification using System Verilog and design test benches

COURSE OUTCOMES: After completion of the course, students should be able to
CO-1: Verify increasingly complex designs more efficiently and effectively
CO-2: Interpret flexible and reliable SV Verification environment, whose components can be re-used across multiple projects
CO-3: Utilize randomization and OOP concepts of SV to build complex digital systems

LIST OF EXPERIMENTS:

Implementation of the following designs using CAD Tools:

1. For the following Designs, develop System Verilog Code and test bench with randomized test vectors then connect the modules using System Verilog interfaces that consist of clocking blocks and mod ports. Verify the functionality and analyze the coverage report.
   a) function f (A, B, C, D) =∑ {0,2,3,5,7} using 4X1 Multiplexer.
   b) 4 to 16 decoder.
   c) 3-bit ALU.
   d) 4-bit up/down-counter.
   e) 4-bit Universal shift register.
   f) 4-bit synchronous SISO shift register.
   g) 2-port arbiter.
   h) Sequence Detector

2. Implement the complete DFT flow (DFT Scan, DFT Insertion, Building Scan Chain and ATPG) for the following Designs
   a) 4-bit Linear feedback shift register
   b) 1100 overlapping mealy sequence
   c) 1001 or 0110 non overlapping mealy sequence
   d) ALU with 8 operations (4 Logical / 4 Arithmetic)

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M.Tech. II Semester (VLSI)	**L**	**T/P**	**C**
	0	**4**	**2**

(A18PW4VS02) MINI-PROJECT

COURSE OUTCOMES: After completion of the course, students should be able to
CO-1: Understand the formulated industry / technical / societal problems
CO-2: Analyze and / or develop models for providing solution to industry / technical / societal problems
CO-3: Interpret and arrive at conclusions from the project carried out
CO-4: Demonstrate effective communication skills through oral presentation
CO-5: Engage in effective written communication through project report

COURSE OUTLINE:

- A student shall undergo a mini-project during II semester of the M.Tech. programme.
- A student, under the supervision of a faculty member, shall collect literature on an allotted project topic of his / her choice, critically review the literature, carry out the mini-project, submit it to the department in a prescribed report form.
- Evaluation of the mini-project shall be done by a Project Review Committee (PRC) consisting of the Head of the Department, faculty supervisor and a senior faculty member of the specialization / department.
- Prior to the submission of mini-project report to the PRC, its soft copy shall be submitted to the PG Coordinator for PLAGIARISM check.
- The mini-project report shall be accepted for submission to the PRC only upon meeting the prescribed similarity index.

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M.Tech. II Semester (VLSI)	**L**	**T/P**	**C**
	2	**0**	**0**

(A18AU5EN01) ENGLISH FOR ACADEMIC AND RESEARCH WRITING

COURSE OBJECTIVES:

- To understand the usage of appropriate vocabulary (Formal, Informal, Gender Insensitive etc.)
- To understand the features and processes of academic writing
- To identify the resources
- To understand standard documentation styles

COURSE OUTCOMES: After completion of the course, students should be able to

CO-1: Use appropriate vocabulary (Formal, Informal, Slang, Gender Insensitive etc.)

CO-2: Employ processes of academic writing

CO-3: Identify the resources

CO-4: Understand standard documentation styles

UNIT- I:

Introduction to Research:

i. Identifying the topic
ii. Identifying Sources; Finding Sources
iii. Defining the broad area; Defining the specific area; Difference between a broad area and specific area
iv. Choosing a topic
v. Mechanics of Writing – Language, Tone, Style, Ethics

UNIT-II:

Referencing & Library Skills:

i. Literature Survey
ii. Writing Objectives
iii. Hypothesis
iv. Methodology
v. Prospects for Future Research

UNIT-III:

Academic Writing Skills:

i. Paraphrasing
ii. Summarizing
iii. Quoting
iv. Rewriting
v. Expansion

UNIT-IV:

Kinds of Academic Writing:

i. Essays
ii. Reports
iii. Reviews
iv. SOPs
v. Abstracts
vi. Proposals

UNIT-V:

Research Process:

i. Selection of Topic

ii. Formulation of Hypothesis
iii. Collection of Data
iv. Analysis of Data
v. Interpretation of Data
vi. Presentation of Data

UNIT-VI:

i. Title
ii. Abstract
iii. Introduction
iv. Literature Survey
v. Methodology
vi. Discussion
vii. Findings/Results
viii. Conclusion
ix. Documenting Sources

TEXT BOOKS:

1. Writing for Science, Goldbort R., Yale University Press (available on Google Books), 2006
2. Handbook of Writing for the Mathematical Sciences, Highman N., SIAM. Highman's Book, 1998

REFERENCES:

1. How to Write and Publish a Scientific Paper, Day R., Cambridge University Press, 2006
2. English for Writing Research Papers, Adrian Wall Work, Springer New York Dordrecht Heidelberg London, 2011
3. MLA Handbook for Research

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M.Tech. III Semester (VLSI)	**L**	**T/P**	**C**
	3	**0**	**3**

(A18OE1MT01) SELECTED TOPICS IN MATHEMATICS

COURSE PRE-REQUISITES: None

COURSE OBJECTIVES:
- To demonstrate accurate and efficient use of specific techniques from the mathematical sciences
- To demonstrate capacity for mathematical reasoning through analyzing, proving and explaining concepts from the mathematical sciences
- To formulate and solve some of problems in natural sciences and engineering by using probabilistic setup

COURSE OUTCOMES: After completion of the course, students should be able to
CO-1: Characterize and represent data collected from experiments using statistical methods
CO-2: Model physical process/systems with multiple variables towards parameter estimation and prediction
CO-3: Represent systems/architectures using graphs and tree towards optimized objective

UNIT-I:
Probability and Statistics: Conditional probability, Bayes Theorem and independent events. Random Variables: Discrete, continuous and mixed random variables, probability mass, probability density and cumulative distribution functions, mathematical expectation, moments, moment generating function, Chebyshev inequality.

UNIT-II:
Special Distributions: uniform, Binomial, Geometric, Poisson, Exponential, Gamma, Normal distributions-Pseudo random sequence generation with given distribution, Functions of a Random Variable

UNIT-III:
Joint Distributions: Joint, marginal and conditional distributions, product moments, correlation, independence of random variables, bi-variate normal distribution.- Stochastic Processes: Definition and classification of stochastic processes, Poisson process - Norms, Statistical methods for ranking data

UNIT-IV:
Multivariate Data Analysis- Linear and non-linear models, Regression Prediction and Estimation, Design of Experiments – factorial method - Response surface method

UNIT-V:
Graphs and Trees: Graphs: Basic terminology, multi graphs and weighted graphs, paths and circuits, shortest path Problems, Euler and Hamiltonian paths and circuits, factors of a graph, planar graph and Kuratowski's graph and theorem, independent sets, graph coloring

UNIT-VI:
Trees: Rooted trees, path length in rooted trees, binary search trees, spanning trees and cut set, theorems on spanning trees, cut sets , circuits, minimal spanning trees, Kruskal's and Prim's algorithms for minimal spanning.

REFERENCES:
1. Probability and Random Process with Applications to Signal Processing, Henry Stark, John W. Woods, 3rd Edition, Pearson Education, 2003

2. Elements of Discrete Mathematics, C. L. Liu, 2nd Edition, Tata McGraw-Hill, 1999
3. Introduction to Linear Regression Analysis, Douglas C. Montgomery, E.A. Peck and G. G. Vining, John Wiley and Sons, 2001
4. Design and Analysis of Experiments, Douglas C. Montgomery, John Wiley and Sons, 2001
5. Random Phenomena: Fundamentals of Probability and Statistics for Engineers, B. A. Ogunnaike, CRC Press, 2010

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M.Tech. III Semester (VLSI)	**L**	**T/P**	**C**
	3	**0**	**3**

(A18PE1VS10) VLSI SIGNAL PROCESSING

COURSE PRE-REQUISITES: Concepts of Signals and Systems, Digital Signal Processing and Basic VLSI Systems

COURSE OBJECTIVES:
- To study various DSP algorithms and retiming concepts
- To learn the concepts of folding and unfolding techniques
- To understand the concepts of systolic architecture design and fast convolution methods
- To describe various power consumption methods in VLSI

COURSE OUTCOMES: After completion of the course, students should be able to
CO-1: Design the systems by using the appropriate DSP algorithms
CO-2: Analyze and design the folding and unfolding techniques in real time application
CO-3: Design the systems by using systolic architectures and various fast convolution algorithms
CO-4: Evaluate the performance of various digital signal processors in terms of low power dissipation

UNIT-I:
Introduction to DSP: Typical DSP algorithms, DSP algorithms benefits, Representation of DSP algorithms
Pipelining and Parallel Processing: Introduction, Pipelining of FIR Digital filters, Parallel Processing, Pipelining and Parallel Processing for Low Power
Retiming: Introduction – Definitions and Properties – Solving System of Inequalities – Retiming Techniques

UNIT-II:
Folding: Introduction -Folding, Transform – Register minimization Techniques – Register minimization in folded architectures – folding of multirate systems

UNIT-III:
Unfolding: Introduction – An Algorithm for Unfolding – Properties of Unfolding – critical Path, Unfolding and Retiming – Applications of Unfolding

UNIT-IV:
Systolic Architecture Design: Introduction – Systolic Array Design Methodology – FIR Systolic Arrays – Selection of Scheduling Vector – Matrix Multiplication and 2D Systolic Array Design – Systolic Design for Space Representations contain Delays

UNIT-V:
Fast Convolution: Introduction – Cook-Toom Algorithm – Winogard algorithm – Iterated Convolution – Cyclic Convolution – Design of Fast Convolution algorithm by Inspection

UNIT-VI:
Low Power Design: Scaling Vs Power Consumption –Power Analysis, Power Reduction techniques – Power Estimation Approaches Programmable DSP: Evaluation of Programmable Digital Signal Processors, DSP Processors for Mobile and Wireless Communications, Processors for Multimedia Signal Processing.

TEXT BOOKS:

1. VLSI Digital Signal Processing- System Design and Implementation, Keshab K. Parhi, Wiley Inder Science, 1998
2. VLSI and Modern Signal Processing, Kung S. Y., H. J. While House, T. Kailath, Prentice Hall, 1985

REFERENCES:

1. Design of Analog – Digital VLSI Circuits for Telecommunications and Signal Processing, Jose E. France, Yannis Tsividis, Prentice Hall, 1994
2. VLSI Digital Signal Processing, Medisetti V. K., IEEE Press (NY), USA, 1995

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M.Tech. III Semester (VLSI)	**L**	**T/P**	**C**
	3	**0**	**3**

(A18PE1VS11) NANOMATERIALS AND NANOTECHNOLOGY

COURSE PRE-REQUISITES: Quantum Physics

COURSE OBJECTIVES:
- To learn the basics of nanotechnology
- To demonstrate understanding characterization techniques for nano materials
- To develop the knowledge of various nanotechnology techniques
- To distinguish various individual nanotech implementations

COURSE OUTCOMES: After completion of the course, students should be able to
CO-1: Understand the basic physics behind the design and fabrication of nano scale systems
CO-2: Understand and formulate new engineering solutions for device applications
CO-3: Make inter disciplinary projects applicable to wide areas in the system development
CO-4: Know the fabrication and characterization of devices for electronic applications

UNIT-I:
Introduction of nanomaterials and nanotechnologies, Features of nanostructures, Applications of nanomaterials and technologies.
Nano dimensional Materials 0D, 1D, 2D structures – Size Effects – Fraction of Surface Atoms – specific Surface Energy and Surface Stress – Effect on the Lattice Parameter – Phonon Density of States – the General Methods available for the Synthesis of Nanostrutures – precipitative – reactive – hydrothermal/solvo thermal methods – suitability of such methods for scaling – potential Uses.

UNIT-II:
Fundamentals of nanomaterials, Classification, Zero-dimensional nanomaterials, One-dimensional nanomaterials, Two-dimensional nanomaterials, Three dimensional nanomaterials. Low-Dimensional Nanomaterials and its Applications, Synthesis, Properties, and Applications of Low-Dimensional Carbon-Related Nanomaterials.

UNIT-III:
Micro- and Nanolithography Techniques, Emerging Applications
Introduction to Micro electro mechanical Systems (MEMS), Advantages and Challenges of MEMS, Fabrication Technologies, Surface Micromachining, Bulk Micromachining, Molding.
Introduction to Nano Phonics.

UNIT 1V:
Introduction, Synthesis of CNTs - Arc-discharge, Laser-ablation, Catalytic growth, Growth mechanisms of CNT's - Multi-walled nanotubes, Single-walled nanotubes Optical properties of CNT's, Electrical transport in perfect nanotubes, Applications as case studies. Synthesis and Applications of CNT's.

UNIT-V:
Nanotechnology for waste reduction and improved energy efficiency, nanotechnology based water treatment strategies. Nanoporous polymers and their applications in water purification, Nanotoxicology. Use of nanoparticles for environmental remediation and water treatment. Case studies and Regulatory needs.

UNIT-VI:
Ferroelectric materials, coating, molecular electronics and nanoelectronics, biological and environmental, membrane based application, polymer based application.

TEXT BOOKS:

1. Nanoscale Materials in Chemistry, Kenneth J. Klabunde and Ryan M. Richards, 2nd Edition, John Wiley and Sons, 2009
2. Nanocrystalline Materials, I. Gusev and A. A. Rempel, 1st Indian Edition, Cambridge International Science Publishing, Viva Books Pvt. Ltd., 2008
3. Nanoscience and Nanotechnology, B. S. Murty, P. Shankar, Baldev Raj, B. B. Rath, James Murday, Tata McGraw Hill Education, 2012

REFERENCES:

1. Springer Handbook of Nanotechnology, Bharat Bhushan, 3rd Edition, Springer, 2010
2. Carbon Nanotubes: Synthesis, Characterization and Applications, Kamal K. Kar, 1st Edition, Research Publishing Services, 2011, ISBN-13: 978-9810863975

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M.Tech. III Semester (VLSI)	**L**	**T/P**	**C**
	3	**0**	**3**

(A18OE1CN01) BUSINESS ANALYTICS

COURSE OBJECTIVES:

- To understand the role of business analytics within an organization and to analyze data using statistical and data mining techniques and understand relationships between the underlying business processes of an organization
- To gain an understanding of how managers use business analytics to formulate and solve business problems and to support managerial decision making and to become familiar with processes needed to develop, report, and analyze business data
- To use decision-making tools/Operations research techniques and to manage business process using analytical and management tools
- To analyze and solve problems from different industries such as manufacturing, service, retail, software, banking and finance, sports, pharmaceutical, aerospace etc.

COURSE OUTCOMES: After completion of the course, students should be able to
CO-1: Apply knowledge of data analytics
CO-2: Think critically in making decisions based on data and deep analytics
CO-3: Use technical skills in predicative and prescriptive modeling to support business decision-making
CO-4: Translate data into clear, actionable insights

UNIT-I:
Business Analytics: Overview of Business analytics, Scope of Business analytics, Business Analytics Process, Relationship of Business Analytics Process and organization, competitive advantages of Business Analytics.
Statistical Tools: Statistical Notation, Descriptive Statistical methods, Review of probability distribution and data modelling, sampling and estimation methods overview.

UNIT-II:
Trendiness and Regression Analysis: Modelling Relationships and Trends in Data, simple Linear Regression. Important Resources, Business Analytics Personnel, Data and models for Business analytics, problem solving, Visualizing and Exploring Data Business Analytics Technology.

UNIT-III:
Organization Structures of Business analytics, Team management, Management Issues, Designing Information Policy, Outsourcing, Ensuring Data Quality, Measuring contribution of Business analytics, Managing Changes.
Descriptive Analytics, predictive analytics, predicative Modelling, Predictive analytics analysis, Data Mining, Data Mining Methodologies, Prescriptive analytics and its step in the business analytics Process, Prescriptive Modelling, nonlinear Optimization.

UNIT-IV:
Forecasting Techniques: Qualitative and Judgmental Forecasting, Statistical Forecasting Models, Forecasting Models for Stationary Time Series, Forecasting Models for Time Series with a Linear Trend, Forecasting Time Series with Seasonality, Regression Forecasting with Casual Variables, Selecting Appropriate Forecasting Models.
Monte Carlo Simulation and Risk Analysis: Monte Carle Simulation Using Analytic Solver Platform, New-Product Development Model, Newsvendor Model, Overbooking Model, Cash Budget Model.

UNIT-V:

Decision Analysis: Formulating Decision Problems, Decision Strategies without Outcome Probabilities, Decision Trees, The Value of Information, Utility and Decision Making.

UNIT-VI:

Recent trends in Embedded and collaborative business intelligence, Visual data recovery, Data Storytelling and Data journalism.

TEXT BOOKS:

1. Business Analytics-Principles, Concepts, and Applications, Marc J. Schniederjans, Dara G. Schniederjans, Christopher M. Starkey, Pearson FT Press
2. Business Analytics, James Evans, Pearson Education
3. Business Analytics, Purba Halady Rao, PHI, 2013

REFERENCES:

1. Business Analytics for Managers: Taking Business Intelligence Beyond Reporting, Gert H. N. Laursen, Jesper Thorlund, 2nd Edition, Wiley Publications
2. Business Analytics: Data Analysis & Decision Making, S. Christian Albright, Wayne L. Winston 5th Edition, 2015
3. Business Intelligence Guidebook: From Data Integration to Analytics, Rick Sherman Elsevier, 2014

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M.Tech. III Semester (VLSI)	**L**	**T/P**	**C**
	3	**0**	**3**

(A18OE1AM01) INDUSTRIAL SAFETY

COURSE PRE-REQUISITES: Elements of Mechanical, Civil, Electrical and Industrial Engineering

COURSE OBJECTIVES:

- To achieve an understanding of principles, various functions and activities of safety management
- To communicate effectively information on Health safety and environment facilitating collaboration with experts across various disciplines so as to create and execute safe methodology in complex engineering activities
- To anticipate, recognize, and evaluate hazardous conditions and practices affecting people, property and the environment, develop and evaluate appropriate strategies designed to mitigate risk
- To develop professional and ethical attitude with awareness of current legal issues by rendering expertise to wide range of industries

COURSE OUTCOMES: After completion of the course, students should be able to

CO-1: Apply risk management principles to anticipate, identify, evaluate and control physical, chemical, biological and psychosocial hazards

CO-2: Communicate effectively on health and safety matters among the employees and with society at large

CO-3: Demonstrate the use of state-of-the-art occupational health and safety practices in controlling risks of complex engineering activities and understand their limitations

CO-4: Interpret and apply legislative / Legal requirements, industry standards, and best practices in accident prevention programmes in a variety of workplaces

UNIT-I:

Safety Management: Evaluation of modern safety concepts – Safety management functions – safety organization, safety department – safety committee, safety audit - performance measurements and motivation – employee participation in safety and productivity.

UNIT-II:

Operational Safety: Hot metal Operation – Boiler, pressure vessels – heat treatment shop - gas furnace operation-electroplating-hot bending pipes – Safety in welding and cutting. Cold-metal Operation- Safety in Machine shop-Cold bending and chamfering of pipes – metal cutting – shot blasting, grinding, painting – power press and other machines

UNIT-III:

Safety Measures: Layout design and material handling - Use of electricity – Management of toxic gases and chemicals – Industrial fires and prevention – Road safety– Safety of sewage disposal and cleaning – Control of environmental pollution – Managing emergencies in industrial hazards.

UNIT-IV:

Accident Prevention: Human side of safety – personal protective equipment – Causes and cost of accidents. Accident prevention programmes - Specific hazard control strategies - HAZOP – Training and development of employees – First Aid – Firefighting devices – Accident reporting investigation.

UNIT-V:

Safety, Health, Welfare & Laws: Safety and health standards – Industrial hygiene – occupational diseases prevention - Welfare facilities – History of legislations related to safety–

pressure vessel act- Indian boiler act- The environmental protection act – Electricity act - Explosive act.

UNIT-VI:

Safe Handling and Storage: Material Handling, Compressed Gas Cylinders, Corrosive Substances, Hydrocarbons, Waste Drums and Containers

TEXT BOOKS:

1. Safety Management, John V. Grimaldi and Rollin H. Simonds, All India Travellers Bookseller, New Delhi, 1989.
2. Safety Management in Industry, Krishnan N. V., Jaico Publishing House, 1996.

REFERENCES:

1. Occupational Safety Manual, BHEL
2. Industrial Safety and The Law, P. M. C. Nair Publisher's, Trivandrum
3. Managing Emergencies in Industries, Loss Prevention of India Ltd., Proceedings, 1999
4. Safety Security and Risk Management, U. K. Singh & J. M. Dewan, A. P. H. Publishing Company, New Delhi, 1996
5. Industrial Safety Management: Hazard Identification and Risk Control, L. M. Deshmukh, McGraw-Hill Education (India) Private Limited, 2005

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M.Tech. III Semester (VLSI)	**L**	**T/P**	**C**
	3	**0**	**3**

(A18OE1AM02) OPERATIONS RESEARCH

COURSE PRE-REQUISITES: Mathematics, Industrial Engineering

COURSE OBJECTIVES:
- To analyze linear programming models in practical and their practical use
- To apply the transportation, assignment and sequencing models and their solution methodology for solving problems
- To apply the theory of games, replacement, inventory and queuing models and their solution methodology for solving problems
- To evaluate the dynamic programming and simulation models

COURSE OUTCOMES: After completion of the course, students should be able to
CO-1: Apply and solve the dynamic programming problems
CO-2: Apply the concept of non-linear programming
CO-3: Carry out sensitivity analysis
CO-4: Model the real world problem and simulate it

UNIT-I:
Introduction to Operations Research-Definitions of OR, Characteristics of OR, Scope of OR, Classification of Optimization Techniques, models in OR, General L.P Formulation, Graphical solution, Simplex Techniques.

UNIT-II:
Revised simplex method - duality theory - dual simplex method – sensitivity or post optimality analysis - parametric programming

UNIT-III:
Nonlinear programming problem - Kuhn-Tucker condition, min cost flow problem - max flow problem - CPM/PERT

UNIT-IV:
Scheduling and sequencing, Inventory models, deterministic inventory, models - Probabilistic inventory control models - Geometric Programming.

UNIT-V:
Waiting line Models, Single and Multi-channel Problems, Dynamic Programming, Game Theory, Simulation.

UNIT-VI:
Introduction to Genetic Algorithms, Operators, applications to engineering optimization, Problems.

TEXT BOOKS:
1. Operations Research, S. D. Sharma, Kedarnath Ramnath, Meerut, New Delhi
2. Engineering Optimization, S. S. Rao, New Age International Publications, 2014
3. Introduction to Genetic Algorithms, S. N. Sivanandam, Springer

REFERENCES:
1. Operations Research-An Introduction, H. A. Taha, PHI, 2008
2. Principles of Operations Research, H. M. Wagner, PHI, Delhi, 1982
3. Introduction to Optimization: Operations Research, J. C. Pant, Jain Brothers, Delhi, 2008

4. Operations Research, Hitler Liebermann McGraw-Hill Pub., 2009
5. Operations Research, Pannerselvam, Prentice Hall of India, 2010

VNR VIGNANA JYOTHI INSTITUTE OF ENGINEERING AND TECHNOLOGY

M.Tech. III Semester (VLSI)	**L**	**T/P**	**C**
	3	**0**	**3**

(A18OE1AM03) COMPOSITE MATERIALS

COURSE PRE-REQUISITES: Maths, Physics, Chemistry, Engineering Mechanics, Mechanics of Solids

COURSE OBJECTIVES:
- To understand composite materials and their properties, relationship between them and manufacturing methods
- To understand the principles of material science applied to composite materials
- To study the equations to analyze problems by making good assumptions and learn systematic engineering methods to solve practical composite mechanics problems

COURSE OUTCOMES: After completion of the course, students should be able to
CO-1: Apply fundamental knowledge of mathematics to modeling and analysis of composite materials
CO-2: Understand the manufacturing methods of various composite materials
CO-3: Analyze the failure modes of composites

UNIT-I:
Introduction: Definition – Classification and characteristics of Composite materials. Advantages and application of composites. Functional requirements of reinforcement and matrix. Effect of reinforcement (size, shape, distribution, volume fraction) on overall composite performance.

UNIT-II:
Reinforcements: Preparation-layup, curing, properties and applications of glass fibers, carbon fibers, Kevlar fibers and Boron fibers. Properties and applications of whiskers, particle reinforcements.
Mechanical Behavior of Composites: Rule of mixtures, Inverse rule of mixtures. Isostrain and Isostress conditions.

UNIT-III:
Manufacturing of Metal Matrix Composites: Casting – Solid State diffusion technique, Cladding – Hot isostatic pressing. Properties and applications.
Manufacturing of Ceramic Matrix Composites: Liquid Metal Infiltration – Liquid phase sintering. Manufacturing of Carbon – Carbon composites: Knitting, Braiding, Weaving. Properties and applications.

UNIT-IV:
Manufacturing of Polymer Matrix Composites: Preparation of Moulding compounds and prepregs – hand layup method – Autoclave method – Filament winding method – Compression moulding – Reaction injection moulding. Properties and applications, Introduction to Machining of Composites.

UNIT-V:
Elastic Behavior of Laminate: Basic assumptions, Strain-displacement relations, Stress-strain relation of layer within a laminate, Force and moment resultant, General load–deformation relations, Analysis of different types of laminates

UNIT-VI:
Strength: Laminar Failure Criteria-strength ratio, maximum stress criteria, maximum strain criteria, interacting failure criteria, hygrothermal failure. Laminate first ply failure-insight

strength; Laminate strength-ply discount truncated maximum strain criterion; strength design using caplet plots; stress concentrations.

TEXT BOOKS:

1. Material Science and Technology, Vol. 13–Composites, R. W. Cahn – VCH, West Germany
2. Analysis and Performance of Fiber Composites, Third Edition, B. D. Agarwal, Wiley Publishers

REFERENCES:

1. Mechanics of Composite Materials, Second Edition. Robert M. Jones, Scripta Book Company
2. Materials Science and Engineering-An Introduction, W. D. Callister Jr., Adapted by R. Bala Subramaniam, John Wiley & Sons, NY, Indian Edition, 2007
3. Composite Materials, K. K. Chawla
4. Composite Materials Science and Applications, Deborah D. L. Chung
5. Composite Materials Design and Applications, Danial Gay, Suong V. Hoa and Stephen W. Tasi

VNR VIGNANA JYOTHI INSTITUTE OF ENGINEERING AND TECHNOLOGY

M.Tech. III Semester (VLSI)	**L**	**T/P**	**C**
	3	**0**	**3**

(A18OE1PS01) WASTE TO ENERGY

COURSE PRE-REQUISITES: None

COURSE OBJECTIVES:
- To create awareness in students of energy conservation
- To identify the use of different types of Bio waste energy resources
- To understand different types of bio waste energy conservations
- To detect different waste conversion into different forms of energy

COURSE OUTCOMES: After completion of the course, students should be able to
CO1: Find different types of energy from waste to produce electrical power
CO2: Estimate the use of bio waste to produce electrical energy
CO3: Understand different types of bio waste and its energy conversions
CO4: Analyze the bio waste utilization to avoid the environmental pollution

UNIT-I:
Introduction to Energy from Waste: Classification of waste as fuel, Agro based, Forest residue, Industrial waste, MSW (Municipal solid waste) – Conversion devices – Incinerators, Gasifiers, Digestors

UNIT-II:
Biomass Pyrolysis: Pyrolysis – Types, slow fast – Manufacture of charcoal – Methods - Yields and application – Manufacture of pyrolytic oils and gases, yields and applications.

UNIT-III:
Biomass Gasification: Gasifiers – Fixed bed system – Downdraft and updraft gasifiers – Fluidized bed gasifiers – Design, construction and operation – Gasifier burner arrangement for thermal heating – Gasifier engine arrangement and electrical power – Equilibrium and kinetic consideration in gasifier operation.

UNIT-IV:
Biomass Combustion: Biomass stoves – Improved chullahs, types, some exotic designs, Fixed bed combustors, Types, inclined grate combustors, Fluidized bed combustors, Design, construction and operation - Operation of all the above biomass combustors.

UNIT-V:
Biogas: Properties of biogas (Calorific value and composition) - Biogas plant technology and status - Bio energy system - Design and constructional features - Biomass resources and their classification - Biomass conversion processes - Thermo chemical conversion - Direct combustion - biomass gasification - pyrolysis and liquefaction - biochemical conversion - anaerobic digestion.

UNIT-VI:
Types of biogas Plants – Applications - Alcohol production from biomass - Bio diesel production - Urban waste to energy conversion - Biomass energy programme in India.

TEXT BOOKS:
1. Biogas Technology-Transfer and Diffusion, M. M. EL-Halwagi, Elsevier Applied Science Publisher, New York, 1984
2. Introduction to Biomass Energy Conversions, Sergio Capareda

REFERENCES:

1. Non-Conventional Energy, Desai Ashok V., Wiley Eastern Ltd., 1990
2. Biogas Technology - A Practical Handbook, Khandelwal, K. C. and Mahdi, S. S., Vol. I & II, Tata McGraw-Hill Publishing Co. Ltd., 1983
3. Food, Feed and Fuel from Biomass, Challal, D. S., IBH Publishing Co. Pvt. Ltd., 1991
4. Biomass Conversion and Technology, C. Y. WereKo-Brobby and E. B. Hagan, John Wiley & Sons, 1996

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M.Tech. III Semester (VLSI)	**L**	**T/P**	**C**
	0	**16**	**8**

(A18PW4VS03) PROJECT PART-I

M.Tech. IV Semester (VLSI)	**L**	**T/P**	**C**
	0	**28**	**14**

(A18PW4VS04) PROJECT PART-II

COURSE OUTCOMES: After completion of the course, students should be able to
CO-1: Identify and formulate the problem (Industry/technical/societal)
CO-2: Analyze, design and develop a solution to industry/technical/societal problems
CO-3: Implement and execute the solution
CO-4: Demonstrate effective communication skills through oral presentation
CO-5: Engage in effective written communication through project report

COURSE OUTLINE:

- M.Tech. project work shall be for a minimum duration of 40 weeks spread over two semesters i.e., Project Part-I in III semester and Project Part-II in IV semester.
- A student shall be permitted to register for the major project after satisfying the attendance requirement in all the courses, i.e., theory and practical courses.
- Project reviews namely Project Review I and Project Review II in III semester and Project Review III and Project Pre-submission Seminar in IV semester shall be conducted during the course of Project work.
- A Project Review Committee (PRC) consisting of the Head of the Department as Chairperson and PG Coordinator, Project Supervisor and one senior faculty member of the Department offering the M. Tech. programme as members shall evaluate the progress of project work.
- In Project Review I, a student, in consultation with his Project Supervisor, shall present the title, objective and plan of action of his/her project work to the PRC for approval within four weeks from the commencement of III semester.
- A student can initiate the project work only after obtaining the approval of the PRC.
- The work on the project shall be initiated at the beginning of the III semester.
- Project Review II shall be conducted and evaluated at the end of the III semester.
- Project Review III shall be conducted during IV semester to examine the overall progress of the project work.
- A project pre-submission seminar shall be conducted to decide whether or not the project is eligible for final submission.
- After approval from the PRC, a soft copy of the thesis shall be submitted for PLAGIARISM check to the Examination Branch.
- At the end of IV semester upon fulfilling the above conditions, project viva-voce shall be conducted.
- A student shall submit project progress in prescribed report format during each of the project reviews.